MT6371 PMIC Datasheet

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Document Revision History

Revision	Date	Author	Description
0.1	2017-08-23	JW Lin	First edition
0.2	2017-11-23	JW Lin	Lists of Figures and Tables Page 5 -Modified table of Contents number Features Page 6, 7 -Modified Charger Voltage Regulation Accuracy condition from 85°C to 70°C Ordering Information Page 11 -Updated the MTK's form Top Marking Definition Page 12 -Updated the MTK's form -Modified DB Output Current from 50mA to 80mA Recommended Operating Range Page20 -Corrected the Supply Input Voltage -Added VBAT Supply Input Voltage Range Electrical Characteristics Page 21, 23, 27, 28, 29, 31 -Corrected VBUS Supply Current Test Conditions -Corrected VBUS Supply Current with PD Communication Test Conditions -Corrected BAT Supply Current SPEC -Modified Parameter description of VOL -Modified Battery Regulation Voltage Accuracy Test Conditions from VOREG_CHG = 4.2v to VOREG = 4.2V, 4.35V, 4.36V or VOREG_CHG = 4.38V -Modified the Parameter description of Strobe CHG_VINOVP -Modified the Parameter description of Strobe CHG_VINOVP Hysteresis -Modified Backlight LED Current Accuracy Test Conditions -Modified Backlight LED Current Matching Test Conditions -Modified Display Bias LDO Dropout Voltage Test Conditions and SPEC -Modified LED Open-Circuit Protection Threshold SPEC -Modified LED Short-Circuit Protection Threshold SPEC -Modified Output Current Limit SPEC -Modified the Test Conditions description of Power Supply Rejection Ratio Application Information Page 35, 49, 54, 84 -Corrected the title from Over-Voltage to Over-Temperature -Deleted the inappropriate description in Interrupt section -Modified the VBUS_DIV2 Measurement Range to 1V to 9.1V -Modified the title name of Figure 3-27 -Modified the title name of Figure 3-28 Functional Descriptions Page 96, 97, 98 -Added more Part Numbers in D1, Q1, L2 position in BOM list

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			-Modified the description of Strobe Mode CHG_VIN OVP in Protection Type Register Table and Descriptions Page 100, 114, 117, 118, 119, 134, 140, 146, 147 -Modified VENDOR_ID from 0101 to 1111 in register table -Modified CHIP_REV from 0001 to 0011 in register table -Removed the DCP STD, CDP and SDP in register table -Modified the description of SDP, SDP NSTD, DCP and CDP -Deleted the 0x71 and 0x77 -Removed the Tracking mode in 0x7A -Modified the description of CHG_VINOVPFL_EVT in Bit Name -Modified the description of CHG_VINOVPFL_STAT in Bit Name -Modified the description of CHG_VINOVPFLM in Bit Name -Added the HVDCPDETM description in 0xE6

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1 Overview

1.1 Features

- **Battery Charger**
  - High-Accuracy Voltage/Current Regulation
  - Average Input Current Regulation (AICR) : 0.1A to 3.25A in 50mA steps
  - Charge Current Regulation Accuracy : ±7%
  - Charge Voltage Regulation Accuracy : ±1% (0 to 70°C)
  - Battery Temperature Sensing
  - Synchronous 1.5Mz/0.75MHz Fixed-Frequency PWM Controller with Up to 95% Duty Cycle
  - Thermal Regulation and Protection
  - Over-Temperature Protection
  - Input Over-Voltage Protection
  - IRQ Output for Communication via I²C
  - Automatic Charging
  - BATFET Control to Support Ship Mode, Wake Up, and Full System Reset
  - Resistance Compensation from Charger Output to Cell Terminal
  - USB OTG Output Voltage Range : 4.425V to 5.825V
  - D+/D- Detection for BC1.2
  - Integrated ADCs for System Monitoring (Charger Current, Voltage, and Temperature)
  - JEITA Thermal Comparator Accuracy ±1% VTS
  - Low Battery Protection from 2.3V to 3.8V for Boost Operation
  - Initial VOREG Set for Relieve Battery Protection
  - External OVP MOSFET Driving for Higher Surge Application, Up to AMR 28V
- **USB_PD**
  - PD-Compatible Dual-Role
  - Attach/Detach Detection as Host, Device or Dual-Role Port
  - Current Capability Definition and Detection
  - Cable Recognition
  - Alternate Mode Supported
  - Supports VCONN with Programmable Over-Current Protection (OCP)
  - Dead Battery Support
  - Ultra-Low Power Mode for Attach Detection (<10mA)
  - BIST Mode Supported
  - USB PD3.0
- **Backlight WLED Driver**
  - Drives up to 4 Strings of 8 series WLEDs
  - External PWM Pin and I2C-Controlled with Programmable 11 bits of Linear and Exponential Brightness
  - I2C-Programmable Over-Voltage Protection (OVP) Threshold
  - Supports Torch Mode and Strobe Mode for Front Cameras
  - Auto Switch Frequency Mode (500kHz, 1MHz)
  - Four Over-Voltage Protection Thresholds (17V, 21V, 25V, and 29V)
  - Four Over-Current Protection Thresholds (900mA, 1200mA, 1500mA, and 1800mA)
  - Front-Facing Flash with 300% Brightness for Selfshot
  - Flash LED Driver
  - Synchronous Boost Dual Flash LED Driver with Dual Independently-Programmable LED Current Sources
  - Torch Mode Current : from 25mA to 400mA in 12.5mA Steps per Channel
  - I2C-Programmable Flash Safety Timer, from 64ms to 2432ms with 32ms/Step
  - Flash LED1/LED2 Short-Circuit

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Protection, and Output Short-Circuit Protection
- TXMask Protection with dedicated FL_TXMASK Pin
- Shared Charger/OTG as Power Stage
- Support Auto-Tracking Mode
- Independent Torch Bypass MOSFET from VSYS
- Strobe Mode Current : 50mA to 1.5A in 12.5mA Steps or 25mA to 750mA in 6.25mA Steps per Channel, and Up to 2.5A in Total

- **Display Bias Driver**
  - I2C-Programmable Output Voltages
  - Flexible Output Voltages (VDB_BST, VDB_POS, VDB_NEG) Setting
  - Boost Converter Output Voltage (VDB_BST) Range : 4V to 6.15V, 50mV/Step
  - Positive Voltage Output (VDB_POS) Range : 4V to 6V, 50mV/Step
  - Negative Voltage Output (VDB_NEG) Range : -4V to -6V, 50mV/Step
  - Selectable Output Mode (Fast Discharge or Float) when Positive/Negative Voltage Output Disabled
  - External Independent Positive/Negative Enable Control
  - True Load Disconnect, Over-Current Protection, and Positive/Negative Short-Circuit Protection Function
  - Output Current : 80mA
  - Power-Saving by Periodic Mode

- **LDO**
  - Output Voltage Range : 1.6V to 4V, 200mV/Step
  - Output Current : 400mA
  - High PSRR and Low Dropout LDO

- **RGB LED Driver**
  - 4-Channel LED Driver
  - Sink Current for 3 RGB LEDs : 24mA/Channel in 4mA Steps
  - PWM Dimming Frequency Range : 0.1Hz to 1kHz
  - RGB_ISINK4 for CHG_VIN Power Good Indicator
  - Support Register Mode, PWM Mode, and Breath Mode

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1.2 Applications

- Cellular Telephones
- Personal Information Appliances
- Tablet PCs
- Portable Instruments

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1.3 General Descriptions

The MT6371 is a highly-integrated smart power management IC, which includes a single cell Li-Ion/Li-Polymer switching battery charger, a USB Type-C & Power Delivery (PD) controller, dual Flash LED current sources, a RGB LED driver, a backlight WLED driver, a display bias driver and a general LDO for portable devices.

The switching charger integrates a synchronous PWM controller, power MOSFETs, input current sensing and input current regulation, high-accuracy voltage regulation, and charge termination circuitry. Besides, the charge current is regulated through the integrated sensing resistors. It also features USB On-The-Go (OTG) support.

The USB Type-C & PD controller complies with the latest USB Type-C and PD standards. It integrates a complete Type-C transceiver including the Type-C termination resistors, Rp and Rd, and enables the USB Type-C detection including attach and orientation. It also integrates the physical layer of the USB BMC power delivery protocol, allowing power transfers and role swaps. The BMC PD function provides full support for alternate modes on the USB Type-C standard.

Dual independent current sources supply for each flash LED. The power for the current sources in strobe mode are from the CHG_VMID pin, which is supplied from the charger in reverse boost mode, the same operation as OTG mode of the charger. The high-side current sources, allowing for grounded-cathode connection for LEDs, provide strobe mode current levels from 25mA to 1.5A in a 12.5 mA step or from 25mA to 750mA in a 6.25mA step and torch mode current levels from 25mA to 400mA in a 12.5mA step. The two channels can support totally up to 2.5A.

The backlight WLED driver supports up to a 29V output voltage for 4 channels of 8 series WLEDs. Each channel supports up to 30mA of current capability with 2048 current steps in exponential or linear mapping curves. The backlight brightness is controlled by the I^2C interface and an external PWM control. The PWM frequency range is from 50Hz to 50kHz. The MT6371 can also support torch/strobe backlight modes with regulated constant current for front camera screen flash applications.

The display bias driver (DB) is implemented with a single-inductor boost and an inverting charge pump to achieve a smaller PCB area, compared with a dual-inductor boost converter. The display bias driver is used to provide a negative voltage output (VDB_NEG) through the DB_NEGVOUT pin and a positive voltage output (VDB_POS) through the DB_POSVOUT pin. The negative voltage output comes from the boost converter output voltage (VDB_BST) at the DB_BSTVOUT pin, and the positive voltage output is from the DB_POSVOUT voltage passing through an LDO to reduce power noise. The VDB_POS and VDB_NEG voltage ranges can be programmed from 4V to 6V and from -4V to -6V with a resolution of 50mV, respectively. These two output rails, usually connected to a Source Driver IC, can support up to 50mA output current capability to drive up to 10" TFT-LCD panels.

The LDO can be used to supply power to an Eccentric Rotating Mass (ERM) Motor in mobile phones and other hand-held devices. The output voltage is programmable in the range of 1.6V to 4V via the I^2C interface.

The RGB LED driver is a 4-Channel smart LED string controller to drive 3 channels of LEDs with a sink current of up to 24mA and a CHG_VIN power good indicator with a sink

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current of up to 6mA. All channels can be set independently via the I^2C interface, and are provided with three operation modes: Register Mode, PWM Mode and Breath Mode.

The MT6371 is available in a WL-CSP-91B 4.22x4.14 (BSC) package.

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1.4 Ordering Information

MT6371□
└Package Type
P : WL-CSP-91B 4.22x4.14 (BSC)

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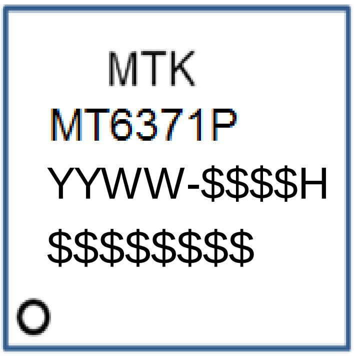
1.5 Top Marking Definition

MT6371P



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1.6 Pin Assignments and Descriptions

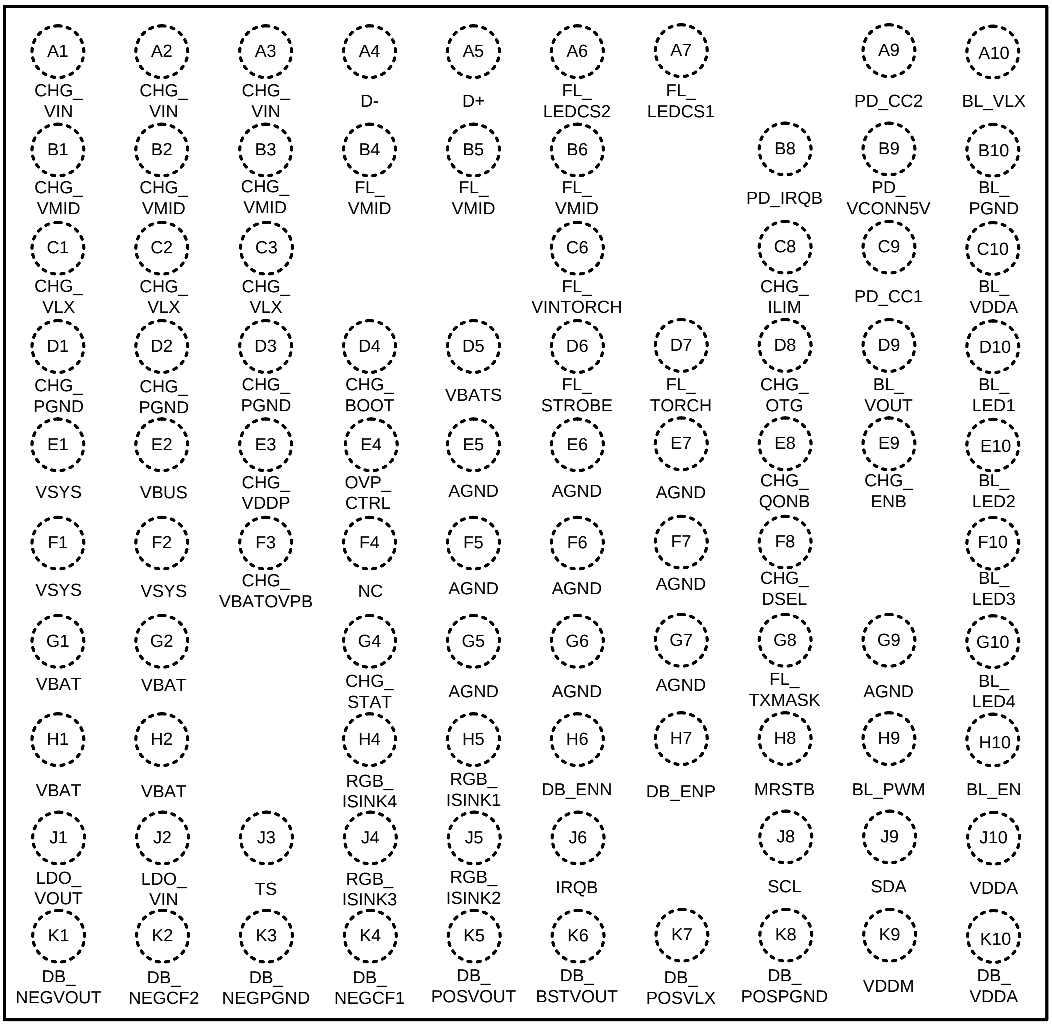

Figure 1-1. MT6371 WL-CSP-91B 4.22x4.14 (BSC) (top view)

Table 1-1. MT6371 pin descriptions

Pin No.	Pin Name	Pin Description
A1, A2, A3	CHG_VIN	Charger power input.
A4	D-	USB D- port.
A5	D+	USB D+ port.
A6	FL_LEDCS2	High-side current source output 2 for flash LED2.
A7	FL_LEDCS1	High-side current source output 1 for flash LED1.
A9	PD_CC2	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation.
A10	BL_VLX	Backlight boost converter switch node. Connect a 10μH inductor between BL_VLX and VSYS.
B1, B2, B3	CHG_VMID	Connection point between the reverse-blocking MOSFET and the high-side switching MOSFET.
B4, B5, B6	FL_VMID	Flash LED driver power input for strobe mode. Connect a 4.7μF ceramic

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Pin No.	Pin Name	Pin Description
		capacitor between FL_VMID and ground.
B8	PD_IRQB	Interrupt output, active-low open-drain, to request the processor to check the registers.
B9	PD_VCONN5V	Regulated input voltage to power PD_CC pins as VCONN.
B10	BL_PGND	Backlight ground. Tie BL_PGND and ground on the PCB.
C1, C2, C3	CHG_VLX	Charger switch node for output inductor connection.
C6	FL_VINTORCH	Flash LED driver power input for torch mode.
C8	CHG_ILIM	Input current limit setting pin. A resistor is connected from CHG_ILIM pin to ground to set the maximum input current limit. The actual input current limit is the lower value set through the CHG_ILIM pin and IAICR register bits.
C9	PD_CC1	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation.
C10	BL_VDDA	Backlight analog power supply. Connect a 1μF ceramic capacitor between BL_VDDA and ground.
D1, D2, D3	CHG_PGND	Charger ground. Tie CHG_PGND and ground on the PCB.
D4	CHG_BOOT	Charger bootstrap voltage to supply the high-side MOSFET gate driver. Connect a capacitor between CHG_BOOT and CHG_VLX.
D5	VBATS	Battery voltage-sense input.
D6	FL_STROBE	Flash LED Strobe mode enable input.
D7	FL_TORCH	Flash LED Torch mode enable input.
D8	CHG_OTG	OTG boost mode enable control, active-high. Act with OTG_Pin_EN (0x11[1]).
D9	BL_VOUT	Backlight output voltage.
D10	BL_LED1	Backlight current regulator output 1.
E1, F1, F2	VSYS	System connection node. Internal BATFET is connected between VSYS and VBAT. Connect a 22μF ceramic capacitor between VSYS and ground.
E2	VBUS	VBUS input voltage for over-voltage protection detection.
E3	CHG_VDDP	Regulated output voltage to supply for the PWM low-side gate driver and the bootstrap capacitor. Connect a 1μF ceramic capacitor CHG_VDDP to ground. 1. If VBUS is plugged in, CHG_VDDP will be powered by VBUS and regulated to 4.9V. 2. If VBUS is unplugged, the charger will operate in sleep mode and the CHG_VDDP voltage will be 0V. * For 2. : Since the CHG_VDDP voltage is also used to power the TS resistor, when the charger is in sleep mode, the CHG_VDDP will be woken up (be reactivated) if VBAT is greater than forward voltage (VF) of the internal high-side (HS) MOS diode by VSLEEP_EXIT with all function of the internal ADC being activated. The CHG_VDDP wake-up time is 500ms.
E4	OVP_CTRL	Input over-voltage protection (IN_OVP) control input.
E5, E6, E7, F5, F6, F7, G5, G6, G7, G9	AGND	Analog ground. Tie AGND and ground on the PCB.
E8	CHG_QONB	Internal BATFET enable control input. In shipping mode, CHG_QONB is pulled Low for the duration of tSHIPMODE_CHG (typical 0.9s) to exit shipping mode.
E9	CHG_ENB	Charger enable input, active-low.
E10	BL_LED2	Backlight current regulator output 2.
F3	CHG_VBATOVP B	Battery over-voltage protection (BAT OVP) indication, open–drain and active-low output: Low if BAT OVP occurs, and High, otherwise.
F4	NC	No internal connection.
F8	CHG_DSEL	Open-drain output. When the device starts to detect input power source, CHG_DSEL drives Low to indicate that detection is in progress and the device needs to take control of the D+ and D- signals. When detection is

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Pin No.	Pin Name	Pin Description
		completed, CHG_DSEL holds Low if DCP (Dedicated Charging Port) or HVDCP adapter is detected. CHG_DSEL returns to High if SDP (Standard Downstream Port) or CDP (Charging Downstream Port) is detected.
F10	BL_LED3	Backlight current regulator output 3.
G1, G2, H1, H2	VBAT	Charge current output node for battery connection. The internal BATFET is connected between VSYS and VBAT. Connect a 10μF ceramic capacitor between VBAT and ground.
G4	CHG_STAT	Charge status indication, open-drain output that indicates charge is in progress when held low and charge is finished when held High. If any fault occurs, CHG_STAT will blink at the frequency of 1Hz. Connect a 2.2k to 10kΩ pull-up resistor.
G8	FL_TXMASK	Configurable power amplifier synchronization input or configurable active-high torch mode enable. Connect an internal pull-down resistor of 300kΩ between FL_TXMASK and ground.
G10	BL_LED4	Backlight current regulator output 4.
H4	RGB_ISINK4	RGB LED current sink output 4.
H5	RGB_ISINK1	RGB LED current sink output 1.
H6	DB_ENN	Enable control input for DB_NEGVOUT.
H7	DB_ENP	Enable control input for DB_POSVOUT.
H8	MRSTB	Manual reset input for hardware reset.
H9	BL_PWM	Backlight PWM dimming control input.
H10	BL_EN	Backlight enable control input.
J1	LDO_VOUT	LDO output. Connect a 2.2μF ceramic capacitor between LDO_VOUT and ground.
J2	LDO_VIN	LDO power input. Connect a 2.2μF ceramic capacitor between LDO_VIN and ground.
J3	TS	Battery temperature-sense input, connected to a resistor divider for temperature programming. If there is no need for the battery temperature-sense function, a 50kΩ resistor is connected to CHG_VDDP and another 50kΩ resistor to ground.
J4	RGB_ISINK3	RGB LED current sink output 3.
J5	RGB_ISINK2	RGB LED current sink output 2.
J6	IRQB	Interrupt output, active-low open-drain, to request the processor to read the registers.
J8	SCL	I2C interface serial clock input. Open-drain. An external pull-up resistor is required.
J9	SDA	I2C interface serial data input/output. Open-drain. An external pull-up resistor is required.
J10	VDDA	Regulated power input for an internal analog base. Connect a 1μF ceramic capacitor between VDDA and ground.
K1	DB_NEGVOUT	Display bias negative voltage output from the inverting charge pump. Connect a 10μF ceramic capacitor between DB_NEGVOUT and ground.
K2	DB_NEGCF2	Inverting charge pump connection point for negative terminal of the flying capacitor. Connect a 10μF ceramic capacitor between DB_NEGCF2 and DB_NEGCF1.
K3	DB_NEGPGND	Display bias negative-voltage power ground. Tie DB_NEGPGND and ground on the PCB.
K4	DB_NEGCF1	Inverting charge pump connection point for positive terminal of the flying capacitor. Connect a 10μF ceramic capacitor between DB_NEGCF2 and DB_NEGCF1.
K5	DB_POSVOUT	Display bias positive voltage output from the LDO. Connect a 10μF ceramic capacitor between DB_POSVOUT and ground.
K6	DB_BSTVOUT	Display bias boost converter output. Connect a 10μF ceramic capacitor between DB_BSTVOUT and ground.

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Pin No.	Pin Name	Pin Description
K7	DB_POSVLX	Display bias boost converter switch node. Connect a 2.2µH inductor between DB_POSVLX and VSYS.
K8	DB_POSPGND	Display bias positive-voltage power ground. Tie DB_POSPGND and ground on the PCB.
K9	VDDM	Regulated voltage output. Connect a 1µF ceramic capacitor between VDDM and PGND. It also provides power to all VDDA-powered circuits.
K10	DB_VDDA	Display bias analog power supply. Connect a 1µF ceramic capacitor between DB_VDDA and ground.

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1.7 Typical Application Circuit

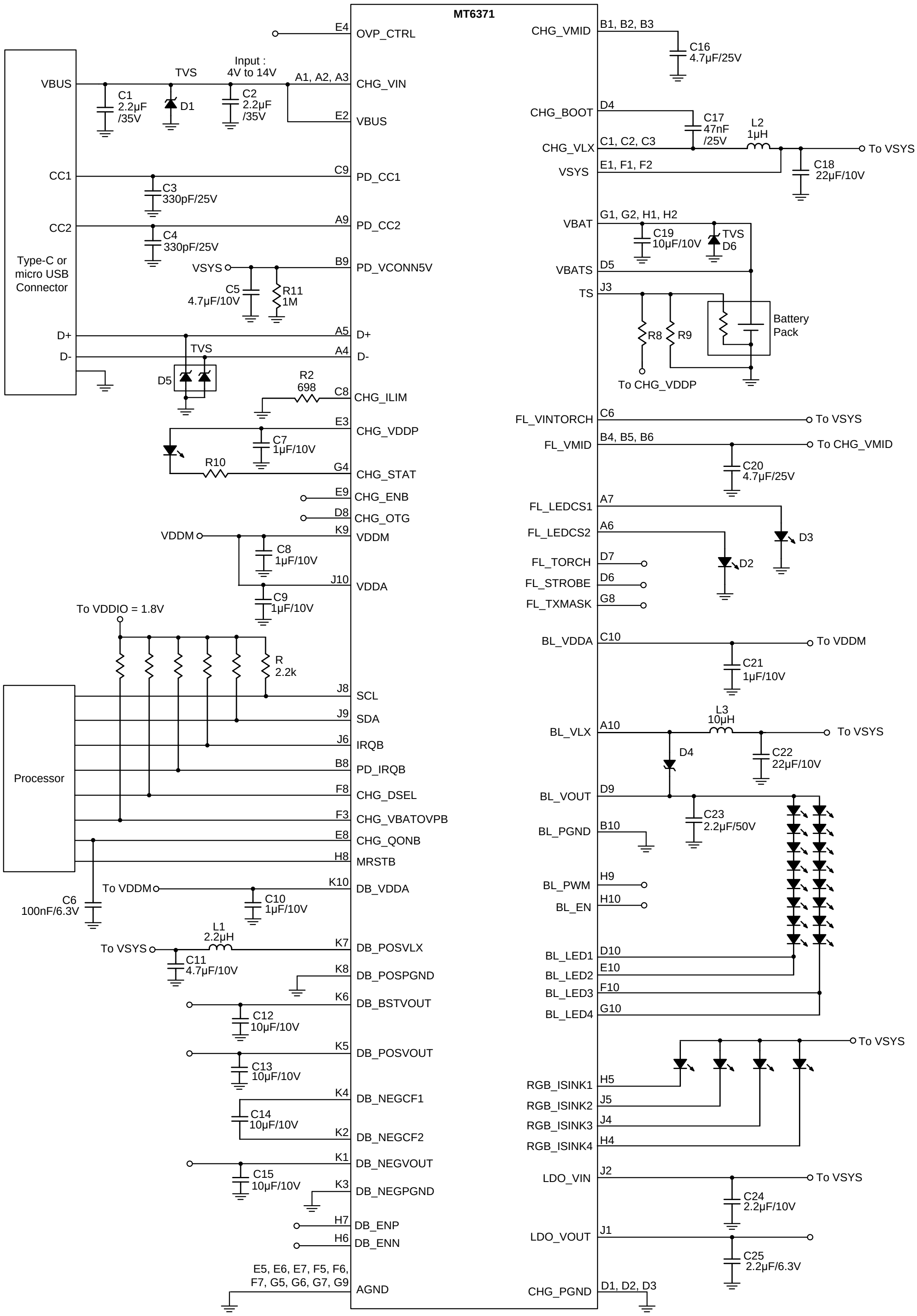

Figure 1-2. Without external OVP function

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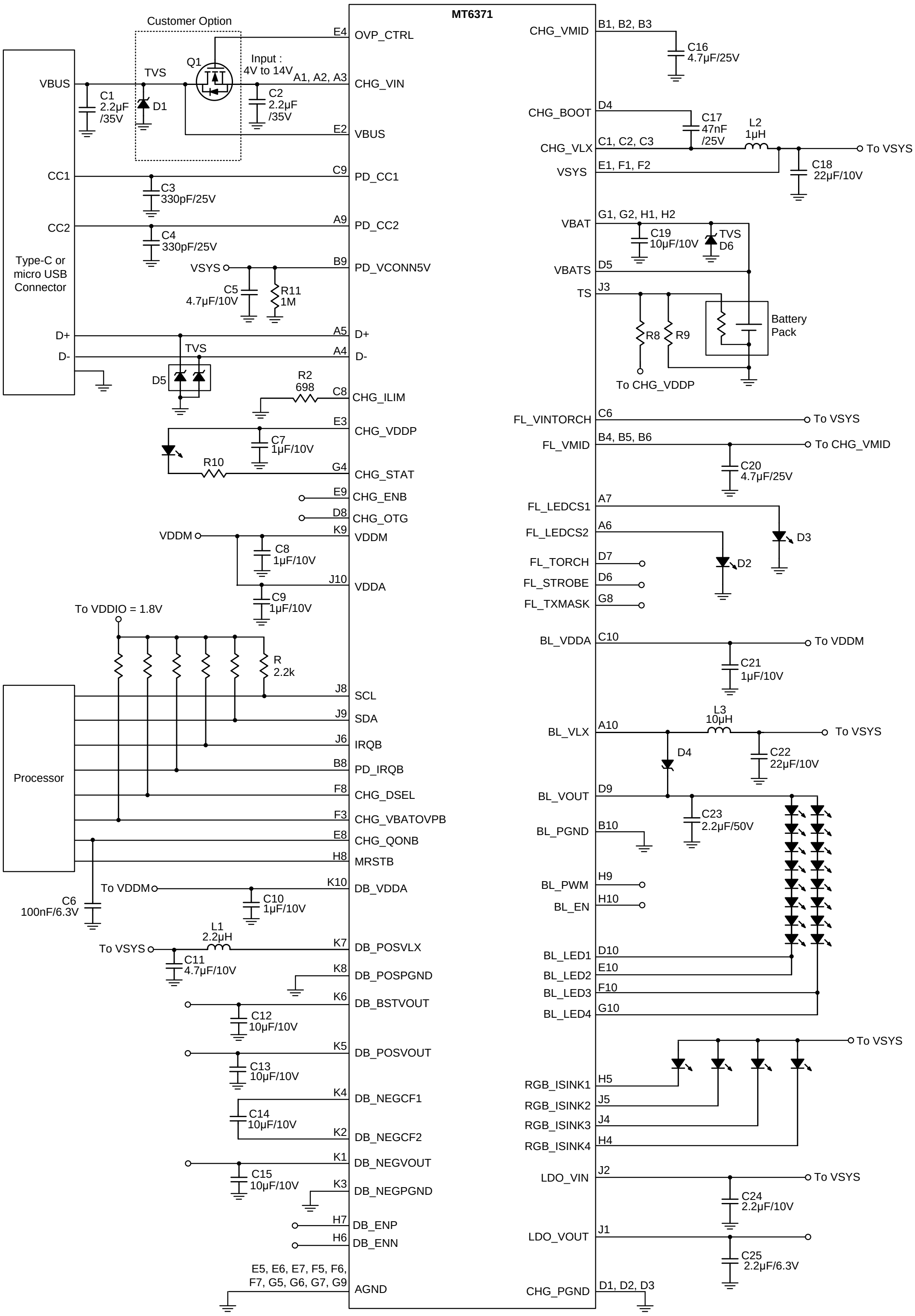

Figure 1-3. With external OVP function

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings

(Note 1)

- BL_VLX, BL_VOUT and (BL_LED1 to BL_LED4) ------------------------------------ -0.3V to 30V
- VBUS -- -0.3V to 28V
- OVP_CTRL, PD_CC1, PD_CC2 -- -0.3V to 24V
- CHG_VIN, CHG_VMID, CHG_BOOT --- -0.3V to 22V
- Negative Charge Pump Switching Voltage (DB_NEGCF2) ---------------------------- 0.3V to -6.5V
- Negative Charge Pump Voltage (DB_NEGVOUT) ------------------------------------ 0.3V to -6.5V
- Other Pins--- -0.3V to 6V
- Power Dissipation, PD @ T_A = 25°C
  WL-CSP-91B 4.22x4.14 (BSC) -- 4.46W
- Package Thermal Resistance (Note 2)
  WL-CSP-91B 4.22x4.14 (BSC), θ_{JA} -- 22.4°C/W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range-- -65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) -- 2kV

Note 1: Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3: Devices are ESD sensitive. Handling precaution recommended.

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2.2 Recommended Operating Range

(Note 4)

- VBUS Supply Input Voltage -- 4V to 14V
- VBAT Supply Input Voltage -- 2.7V to 5.5V
- Junction Temperature Range -- 40°C to 125°C
- Ambient Temperature Range -- -40°C to 85°C

Note 4: The device is not guaranteed to function outside its operating conditions.

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2.3 Electrical Characteristics

V_{CHG_VIN} = 5V, V_{BAT} = 4.2V, L2 = 1μH, C2 = 2.2μF, C19 = 10μF, T_A = 25°C, unless otherwise specified

Table 2-1. Electrical specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current						
Shutdown Current	I_{SHDN}	On VBAT pin, with all channels shut down, V_{BAT} = 4V	--	60	85	μA
Shipping-Mode Current	I_{BAT_SHIP}	VBAT only, in shipping mode	--	31	46	μA
V_{BUS} Supply Current	I_{VBUS}	V_{CHG_VLX} is non-switching, V_{BUS} = 5V, V_{BAT} = V_{CV_CHG}, ICHG = 0, Flash LED, LDO, Backlight and RGB devices disabled, PD Cable attached (Full functions are not in the communication situation)	--	8.55	11.12	mA
V_{BUS} Supply Current with PD Communication	$I_{VBUS_PDTX_ON}$	V_{CHG_VLX} is non-switching, V_{BUS} = 5V, V_{BAT} = V_{CV_CHG}, I_{CHG} = 0, Flash LED, LDO, backlight and RGB drivers disabled, PD Cable attached (Full functions are in the communication situation)	--	12.55	16.31	mA
V_{BUS} Supply Current with Charger in H-Z Mode	I_{VBUS_HZ}	V_{CHG_VLX} is in high-impedance mode, V_{BUS} = 5V, V_{BAT} = V_{CV_CHG} Flash LED, LDO, Backlight and RGB devices disabled, PD in ultra-low power mode	--	810	1053	μA
BAT Supply Current	$I_{BAT_LDO_ON}$	V_{BUS} = 0V, V_{BAT} = 3.8V, charger, Flash LED, Backlight and RGB devices disabled, LDO enabled with load = 0, PD in ultra-low power mode	--	200	300	μA
BAT Supply Current	$I_{BAT_DB_ON}$	V_{BUS} = 0V, V_{BAT} = 3.8V, charger, Flash LED, Backlight and RGB devices disabled, display bias driver enabled with load = 0, PD in ultra-low power mode	--	1750	2100	μA
Over-Temperature Protection Threshold	T_{OTP}	Thermal shutdown threshold temperature	--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	Thermal shutdown hysteresis temperature	--	20	--	°C
Control I/O Pin & VDDA						
Logic-Low Threshold Voltage for All Open-Drain Outputs	V_{OL}	I_{DS} = 10mA	--	--	0.4	V
Logic-High Threshold Voltage for All Inputs	V_{IH}	Logic high threshold	1.2	--	--	V
Logic-Low Threshold Voltage for All Inputs	V_{IL}	Logic low threshold	--	--	0.4	V
VDDA Under-Voltage Protection Threshold	V_{VDDA_UVLO}	V_{DDA} falling	2.5	2.6	2.7	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDA Under-Voltage Protection Hysteresis	$V_{VDDA_UVLO_HYS}$	V_{DDA} rising	--	0.1	--	V
VDDA Over-Voltage Protection Threshold	V_{VDDA_OVP}	V_{DDA} rising	5.25	5.5	5.75	V
VDDA Over-Voltage Protection Hysteresis	$V_{VDDA_OVP_HYS}$	V_{DDA} falling	--	0.2	--	V
Pull-Down Resistance on MRSTB	R_{L_MRSTB}		--	300	--	kΩ
OVP Controller						
VBUS POR Threshold for CHG_VIN Only	V_{POR_OVP}	V_{BUS} rising	2.5	2.7	2.9	V
VBUS POR Hysteresis Only for CHG_VIN	$V_{POR_OVP_HYS}$	V_{BUS} falling	--	100	--	mV
POR Deglitch Time Only for CHG_VIN	$t_{D_POR_OVP}$	V_{BUS} = 5V to 12V	22.4	32	41.6	ms
Over-Voltage Protection Threshold	V_{OVP}	V_{BUS} rising	15.5	16.5	17.5	V
Over-Voltage Protection Hysteresis	V_{OVP_HYS}	V_{BUS} falling	--	200	--	mV
OVP Propagation Delay for MOS Turned Off	t_{PD_OVP}	V_{BUS} from 12V to 20V, (6V/μs), Q_g of MOS at V_{GS} = 4.5V < 20nC	--	0.18	0.25	μs
OVP Recovery Delay	t_{RD_OVP}	V_{BUS} from 20V to 12V	5.6	8	10.4	ms
Charger						
Sleep-Mode Entry Threshold, VBUS-VBAT	$V_{SLEEP_ENTER_CHG}$	V_{BUS} falling, 2.5V < V_{BAT} < V_{OREG_CHG}	0	0.04	0.1	V
Sleep-Mode Exit Threshold, VBUS-VBAT	$V_{SLEEP_EXIT_CHG}$	V_{BUS} rising, 2.5V < V_{BAT} < V_{OREG_CHG}	0.04	0.1	0.2	V
Sleep-Mode Exit Deglitch Time	$t_{D_SLEEP_EXIT_CHG}$	Exit sleep-mode	--	120	--	ms
CHG_VIN Bad Adapter Threshold	$V_{BAD_ADP_CHG}$		--	3.8	--	V
CHG_VIN Bad Adapter Hysteresis	$V_{BAD_ADP_HYS_CHG}$		--	150	--	mV
CHG_VIN Bad Adapter Sink Current	$I_{BAD_ADP_SINK_CHG}$		--	50	--	mA
CHG_VIN Bad Adapter Detection Time	$t_{BAD_ADP_DET_CHG}$		--	30	--	ms
Input Current Limit Factor	K_{ILIM_CHG}	Input current regulation 508mA by ILIM pin with resistance = 698Ω	320	355	390	AΩ
CHG_VIN Minimum Input Voltage Regulation (MIVR) Threshold	V_{MIVR_CHG}	I²C programmable range in 0.1V steps	3.9	--	13.4	V
CHG_VIN Minimum Input Voltage Regulation Accuracy	$V_{MIVR_ACC_CHG}$	V_{MIVR} = 4.4V or 9V	-2	--	2	%

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AICR 100mA Mode	$I_{AICR_100mA_CHG}$	I_{AICR} = 100mA, V_{CHG_VIN} = 5V, VBAT = 3.8V	86	93	100	mA
AICR 500mA Mode	$I_{AICR_500mA_CHG}$	I_{AICR} = 500mA, V_{CHG_VIN} = 5V, VBAT = 3.8V	440	470	500	mA
AICR 1000mA Mode	$I_{AICR_1000mA_CHG}$	I_{AICR} = 1000mA, V_{CHG_VIN} = 5V, VBAT = 3.8V	880	940	1000	mA
AICR 1500mA Mode	$I_{AICR_1500mA_CHG}$	I_{AICR} = 1500mA, V_{CHG_VIN} = 5V, V_{BAT} = 3.8V	1300	1400	1500	mA
CHG_VIN UVLO	V_{UVLO_CHG}	V_{CHG_VIN} rising	3.05	3.3	3.55	V
CHG_VIN UVLO Hysteresis	$V_{UVLO_HYS_CHG}$	V_{CHG_VIN} falling	--	150	--	mV
CHG_VIN Over-Voltage Protection Threshold	$V_{CHG_VIN_OVP_CHG}$	V_{CHG_VIN} rising	13.5	14.5	15.5	V
CHG_VIN Over-Voltage Protection Hysteresis	$V_{CHG_VIN_OVP_HYS_CHG}$	V_{CHG_VIN} falling	--	250	--	mV
VBAT Over-Voltage Protection Threshold	$V_{BAT_OVP_CHG}$	V_{BAT} rising, as percentage of V_{OREG_CHG}, as (V_{BAT_OVP}-V_{OREG_CHG})/V_{OREG_CHG}	106	108	110	%
VBAT Over-Voltage Protection Hysteresis	$V_{BAT_OVP_HYS_CHG}$	V_{BAT} falling, as ($V_{BAT_OVP_HYS}$)/V_{OREG_CHG}	--	4	--	%
Thermal Regulation Threshold	t_{THREG_CHG}	Charge current starts decreasing (default)	--	120	--	°C
VSYS Over-Voltage Protection Threshold	$V_{SYS_OVP_CHG}$	V_{SYS} rising	4.9	5.25	5.5	V
VSYS Under-Voltage Protection	$V_{SYS_UVP_CHG}$	V_{SYS} falling	2.2	2.4	2.6	V
End of Charge						
Battery Regulation Voltage Range	V_{OREG_CHG}	I²C programmable in 10mV steps	3.9	--	4.71	V
Battery Regulation Voltage Accuracy	$V_{OREG_ACC_CHG}$	V_{OREG_CHG} = 4.2V, 4.35V, 4.36V, 4.37V or V_{OREG_CHG} = 4.38V (T_C = 0°C to 70°C) (Note 7)	-0.5	--	0.5	%
Re-charge Mode Threshold	V_{RECH_CHG}	I²C programmable, V_{BAT} falling, the difference below V_{OREG_CHG}	50	100	150	mV
Re-charge Deglitch Time	$t_{D_RECH_CHG}$	V_{BAT} falling	--	120	--	ms
End-of-charge Current	I_{EOC_CHG}	I²C programmable in 50mA steps	100	--	850	mA
Default End-of-charge Current	$I_{EOC_DEF_CHG}$	Default.	--	250	--	mA
End-of-charge Current Accuracy	I_{EOC_ACC}	I_{EOC_CHG} = 100 to 850mA	-20	--	20	%
End-of-charge Deglitch Time	$t_{D_EOC_CHG}$	I²C default, I_{CHG} < I_{EOC_CHG}, V_{BAT} > V_{RECH_CHG}	--	2	--	ms
Charge Current	I_{CHG}	I²C programmable in 0.1A steps, 0x17 bit[7:2]	0.5	--	5	A
ICHG Current Accuracy 1	$I_{CHG_ACC1_CHG}$	V_{BAT} = 3.8V, I_{CHG} = 500mA, (T_C = -30°C to 65°C)	-20	--	20	%
ICHG Current Accuracy 2	$I_{CHG_ACC2_CHG}$	V_{BAT} = 3.8V, 500mA < I_{CHG} < 1000mA, (T_C = -30°C to 65°C)	-10	--	10	%

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ICHG Current Accuracy 3	$I_{CHG_ACC3_CHG}$	V_{BAT} = 3.8V, I_{CHG} > 1000mA, (T_C = -30°C to 65°C)	-7	--	7	%
Pre-Charge Mode Threshold	V_{PRECHG_CHG}	I²C programmable in 0.1V steps, rising	2.0	--	3.5	V
Pre-Charge Mode Hysteresis	$V_{PRECHG_HYS_CHG}$	Pre-charge hysteresis, falling	--	0.2	--	V
Pre-Charge Threshold Accuracy	$V_{PRECHG_ACC_CHG}$	$V_{BAT} < V_{PREC_CHG}$	-5	--	5	%
Pre-Charge Current	I_{PRECHG_CHG}	I²C programmable (default)	--	150	--	mA
Pre-Charge Current Accuracy	$I_{PRECHG_ACC_CHG}$		-20	--	20	%
Trickle Charge Threshold	V_{TRICHG}	VBAT falling	--	2	--	V
Trickle Charge Threshold Hysteresis	V_{TRICHG_HYS}	VBAT rising	--	200	--	mV
Trickle Charge Threshold Accuracy	V_{TRICHG_ACC}		-5	--	5	%
Trickle Current	I_{TRICHG}	VBAT < 2V, charge with ICC = 100mA; VBAT < 1.6V, charge with AICR = 100mA	--	100	--	mA
Trickle Current Accuracy	I_{TRICHG_ACC}		-20	--	20	%
V_{SYS} Regulation Voltage	$V_{SYS_MIN_CHG}$	I²C programmable in 0.1V steps	3.3	--	4	V
V_{SYS} Regulation Voltage Accuracy	$V_{SYS_MIN_ACC_CHG}$		-3	--	3	%
UUG On-Resistance	$R_{ON_UUG_CHG}$	From VBUS to CHG_VMID	--	14	30	mΩ
UG On-Resistance	$R_{ON_UG_CHG}$	From CHG_VMID to CHG_VLX	--	28	40	mΩ
LG On-Resistance	$R_{ON_LG_CHG}$	From CHG_VLX to PGND	--	28	40	mΩ
PPMOS On-Resistance	$R_{ON_PPMOS_CHG}$	From VSYS to VBAT	--	13	30	mΩ
Switching Frequency	f_{OSC1_CHG}	I²C programmable to 1.5 MHz	--	1.5	--	MHz
Switching Frequency	f_{OSC2_CHG}	I²C programmable to 0.75MHz	--	0.75	--	MHz
Switching Frequency Accuracy	$f_{OSC_ACC_CHG}$		-10	--	10	%
Maximum Duty Cycle	D_{MAX_CHG}		--	97	--	%
Minimum Duty Cycle	D_{MIN_CHG}		0	--	--	%
VDDP Regulation	V_{VDDP_CHG}	V_{BUS} = 5V	4.5	4.9	5.3	V
Buck OCP Current	$I_{BUCK_OCP_CHG}$	REG0x1D[2] = 1'b0	4	6	8	A
		REG0x1D[2] = 1 'b1	5.6	8	10.4	
Sink Current for Battery Detection	$I_{BAT_SINK_CHG}$		--	300	--	µA
Internal QONB Pull-Up Resistance	R_{QONB_CHG}		90	125	160	kΩ
QONB Exit Shipping Mode Duration	$t_{SHIPMODE_CHG}$	CHG_QONB Low for BATFET on-time to exit shipping mode	0.81	0.9	0.99	s

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
QONB System Reset Duration	$t_{QONB_RST_CHG}$	CHG_QONB low time to enable full system reset	12	15	18	s
BATFET Reset Time	$t_{BATFET_RST_CHG}$	BATFET off-time during full system reset	0.54	0.6	0.66	s
Shipping Mode Entry Deglitch Time	$t_{D_SHIP_ENTER}$	Enter shipping mode delay	--	9	--	s
AICL	V_{AICL_CHG}	V_{BUS} rising, I²C programmable	--	4.6	--	V
AICL Hysteresis	$V_{AICL_HYS_CHG}$		--	50	--	mV
OTG Output Regulation	V_{BSTCV_CHG}	I²C programmable default	--	5.05	--	V
OTG Output Accuracy	$V_{BSTCV_ACC_CHG}$	I_{VBUS} = no load, VOBST = 5.05V	-3	--	3	%
OTG Over-Load Protection Threshold	$I_{BST_0.5A_CHG}$	OTG_OC = 0.5A, 0x1A[2:0] = 000	0.5	--	--	A
OTG CHG_VMID Over-Voltage Protection Threshold	$V_{MIDOVP_OTG_CHG}$	V_{CHG_VMID} rising	4.2	6	--	V
OTG CHG_VMID Over-Voltage Protection Hysteresis	$V_{MIDOVP_OTG_HYS_CHG}$		--	200	--	mV
OTG VBAT Under-Voltage Protection Threshold	$V_{BAT_UVP_OTG_CHG}$	I²C default, VBAT falling	--	2.8	3.08	V
OTG VBAT Under-Voltage Protection Hysteresis	$V_{BAT_UVP_OTG_HYS_CHG}$	Rising	--	400	--	mV
OTG Over-Current Protection Threshold	$I_{OTG_OCP_CHG}$	Default = 6.05A	5.2	6.05	6.9	A
Battery Temperature HOT Threshold	$V_{VTS_HOT_CHG}$	V_{TS} falling, the ratio of CHG_VDDP	33.5	34.5	35.5	%VTS
Battery Temperature WARM Threshold	$V_{VTS_WARM_CHG}$	V_{TS} falling, the ratio of CHG_VDDP	44	45	46	%VTS
Battery Temperature COOL Threshold	$V_{VTS_COOL_CHG}$	V_{TS} rising, the ratio of CHG_VDDP	67.5	68.5	69.5	%VTS
Battery Temperature COLD Threshold	$V_{VTS_COLD_CHG}$	V_{TS} rising, the ratio of CHG_VDDP	72.5	73.5	74.5	%VTS
Battery Temperature Hysteresis	$V_{VTS_HYS_CHG}$		--	2	--	%VTS
VDP_SRC Voltage	$V_{DP_SRC_CHG}$	With IDAT_SRC = 0 to 250μA	0.5	--	0.7	V
VDAT_REF Voltage	$V_{DAT_REF_CHG}$		0.25	--	0.4	V
VLGC Voltage	V_{LGC_CHG}		0.8	--	2	V
IDM SINK Current	IDM_SINK	May be a resistance if desired	50	100	150	μA
Data Contact Timeout	t_{DCDT}	Setting by register 0x22[5:4]	--	600	--	ms
Dedicated Charging Port resistance across D+/-	$R_{D+D-\ DCP}$	sEN_DCP = 1	50	90	130	Ω

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pull-Down Resistance on CHG_OTG	$R_{L_CHG_OTG}$		--	100	--	kΩ
Pull-Up Resistance on CHG_ENB	R_{CHG_ENB}		--	100	--	kΩ
ADC						
ADC Conversion Time	t_{CONV_ADC}	One channel	35	--	200	ms
Number of Bits for ADC Resolution	R_{ES_ADC}		--	10	--	bits
VBUS_DIV5 Measurement Range	$V_{VBUS_DIV5_ADC_RANGE}$		1	--	22	V
VBUS_DIV5 Resolution	$V_{VBUS_DIV5ADC_RES}$		--	25	--	mV
VBUS_DIV5 Accuracy	$V_{VBUS_DIV5ADC_ACC}$		-3	--	3	LSB
VBUS_DIV2 Measurement Range	$V_{VBUS_DIV2_ADC_RANGE}$		1	--	9.7	V
VBUS_DIV2 Resolution	$V_{VBUS_DIV2ADC_RES}$		--	10	--	mV
VBUS_DIV2 Accuracy	$V_{VBUS_DIV2ADC_ACC}$		-3	--	3	LSB
VBAT Measurement Range	$V_{BAT_ADC_RANGE}$		0	--	4.9	V
VBAT Resolution	$V_{BAT_ADC_RES}$		--	5	--	mV
VBAT Accuracy	$V_{BAT_ADC_ACC}$		-2	--	2	LSB
VSYS Measurement Range	$V_{SYS_ADC_RANGE}$		0	--	4.9	V
VSYS Resolution	$V_{SYS_ADC_RES}$		--	5	--	mV
VSYS Accuracy	$V_{SYS_ADC_ACC}$		-2	--	2	LSB
CHG_VDDP Measurement Range	$V_{CHG_VDDP_ADC_RANGE}$		0	--	4.9	V
CHG_VDDP Resolution	$V_{CHG_VDDP_ADC_RES}$		--	5	--	mV
CHG_VDDP Accuracy	$V_{CHG_VDDP_ADC_ACC}$		-2	--	2	LSB
TS_BAT Measurement Range	$R_{ATETS_BAT_RANGE}$		0	--	100	%
TS_BAT Resolution	$R_{ATETS_BAT_RES}$		--	0.25	--	%
TS_BAT Accuracy	$R_{ATETS_BAT_ACC}$		-2	--	2	LSB
IBUS Measurement Range	$I_{BUS_ADC_RANGE}$		0	--	5	A
IBUS Resolution	$I_{BUS_ADC_RES}$		--	50	--	mA
IBUS Accuracy	$I_{BUS_ADC_ACC}$	I_{BUS} > 2A, IAICR [5:0] setting ≥ 400mA	-3	--	3	LSB
		I_{BUS} < 2A, IAICR [5:0] setting ≥ 400mA	-2	--	2	
		I_{BUS} < 2A, IAICR [5:0] setting < 400mA	-2	--	2	
IBAT Measurement Range	$I_{BAT_ADC_RANGE}$		0	--	5	A
IBAT Resolution	$I_{BAT_ADC_RES}$		--	50	--	mA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBAT Accuracy	$I_{IBAT_ADC_ACC}$		-2	--	2	LSB
TEMP_JC Measurement Range	$T_{TEMP_JC_ADC_RANGE}$		-40	--	120	°C
TEMP_JC Resolution	$T_{TEMP_JC_ADC_RES}$		--	2	--	°C
TEMP_JC Accuracy	$T_{TEMP_JC_ADC_ACC}$	Temperature < 85°C	-2	--	2	LSB
Pump Express						
PE+1 On Time (A)	$t_{ON_A_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	430	500	570	ms
PE+1 On Time (B)	$t_{ON_B_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	240	300	360	ms
PE+1 On Time (C)	$t_{ON_C_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	70	100	130	ms
PE+1 Off Time (D)	$t_{OFF_D_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	70	100	130	ms
PE+1 Off Time (I)	$t_{OFF_I_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	80	--	225	ms
PE+2 Off Time (D)	$t_{OFF_D_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	87	105	128	ms
PE+2 On Time (E)	$t_{ON_E_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	147	190	248	ms
PE+2 On Time (F)	$t_{ON_F_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	87	102.5	118	ms
PE+2 On Time (G)	$t_{ON_G_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	22	50	68	ms
PE+2 Off Time (H)	$t_{OFF_H_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	22	50	68	ms
PE+2 Off Time (I)	$t_{OFF_I_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	135	155	175	ms
Flash LED Current Source						
LED Current Accuracy	$I_{LED1_ACC_FL}$	Flash LED current is set 25mA to 400mA	-8	--	8	%
LED Current Accuracy	$I_{LED2_ACC_FL}$	Flash LED current set 0.4A to 1A	-6	--	6	%
FL_LEDCSx Leakage Current	I_{LEAK_FL}	VLEDVIN = 5V, LEDCSX = 0, LEDCSX disabled	--	0.1	4	μA
FL_LEDCSx Start Up Current	I_{START_FL}	LEDCSX = 0, LEDCSX enabled	--	320	1000	μA
LEDCSX Short Threshold	V_{SC_FL}		--	1	1.3	V
LEDCSX Short Event Timer	$t_{D_SC_FL}$		1.8	2.5	3.3	ms
Flash Time-Out	$t_{TIMEOUT_FL}$	FLEDx_STRB_TO = 0100101	--	1248	--	ms
Flash Timer Accuracy	$t_{TMR_ACC_FL}$	Timer set by register	-10	--	10	%
Current Source Regulation Voltage	V_{REG1_FL}	I_{LED} = 200mA, 0x7C[1:0] = 00	--	200	300	mV
Current Source Regulation Voltage	V_{REG2_FL}	I_{LED} = 1500mA, 0x7C[1:0] = 01	--	--	500	mV
Strobe/TXMask Deglitch Time	$t_{D_STRB_FL}$		--	10	--	μs
Flash Ready Time	$t_{FLSH_RDY_FL}$	EN_LEDCS = 1 to current reach 800mA target value	--	4.5	5	ms
Strobe FL-CHG_VIN OVP	VIN_OVP_FL		5.45	5.6	5.75	V
Strobe FL-CHG_VIN OVP Hysteresis	VIN_OVP_Hys_FL		0.25	0.3	0.35	V
Timer Accuracy	$t_{D_ACC_FL}$	V_{DDA} = 2.7V to 5.5V (for deglitch time, soft-start)	--	10	15	%
High Side Switch On-Resistance	$R_{ON_H_FL}$		--	60	--	mΩ

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low Side Switch On-Resistance	$R_{ON_L_FL}$		--	36	--	mΩ
Pull-Down Resistance on FL_STROBE	$R_{L_FL_STROBE}$		--	350	--	kΩ
Pull-Down Resistance on BL_EN	$R_{L_FL_TORCH}$		--	350	--	kΩ
Pull-Down Resistance on FL_TXMASK	$R_{L_FL_TXMASK}$		--	300	--	kΩ
Backlight						
Maximum Backlight LED Current	$I_{LED_MAX_BL}$	Maximum LED current (per string)	--	30	--	mA
Backlight LED Current Accuracy	$I_{LED_ACC_BL}$	2.7V ≤ V_{SYS} ≤ 5V, 6mA < I_{LED} < 30mA, Linear or Exponential Mode	-3	--	3	%
		2.7V ≤ V_{SYS} ≤ 5V, 0.1mA < I_{LED} < 6mA, Linear or Exponential Mode	-10	--	10	%
Backlight LED Current Matching	$I_{LED_MATCH_BL}$	2.7V ≤ V_{SYS} ≤ 5V, 100μA < I_{LED} < 30mA, Linear or Exponential Mode	-3	0.2	3	%
Minimum Backlight LED Current	$I_{LED_MIN_LINEAR_BL}$	PWM or I²C current control linear mode (per string) (Note 7)	--	14.6	--	μA
Minimum Backlight LED Current	$I_{LED_MIN_EXP_BL}$	PWM or I²C current control exponential mode (Note 7)	--	60	--	μA
LED Current Step size	$I_{LED_STEP_EXP_BL}$	Exponential mode (Code to Code)	--	0.3	--	%
LED Current Step size	$I_{LED_STEP_LINEAR_BL}$	Linear mode (Code to Code)	--	14.6	--	μA
Backlight Output Over-Voltage Protection Threshold	V_{OVP_BL}	2.7V ≤ VCHG_VIN ≤ 5V, rising. BLED_OVP @ REG0xA1[6:5] = 2'b01	19.8	21	22.2	V
Regulated Current Sink Headroom Voltage (Boost Feedback Voltage)	V_{HR_BL}	I_{LED} = 3 mA	--	500	--	mV
N-MOSFET On-Resistance	$R_{ON_N_BL}$	I_{SW} = 500mA	--	0.2	--	Ω
Switching Frequency	f_{SW_BL}	2.7V ≤ V_{IN} ≤ 5V	450	500	550	kHz
		2.7V ≤ V_{IN} ≤ 5V	900	1000	1100	kHz
N-MOSFET Current Limit Tolerance	$I_{LIM_NMOS_BL}$	2.7V ≤ V_{IN} ≤ 5V @ REG0xA1[2:1]: BL_OC = 2'b01	960	1200	1440	mA
Maximum Boost Duty Cycle	$D_{MAX_BST_BL}$		92	96	--	%
PWM Input Frequency Range	f_{PWM_BL}	2.7V ≤ V_{IN} ≤ 5V	50	--	50000	Hz
Minimum Pulse ON Time	$t_{ON_MIN_BL}$	Sample rate = 24MHz	183.3	--	--	ns
		Sample rate = 4MHz	1100	--	--	
		Sample rate = 1MHz	5500	-	--	
Minimum Pulse OFF Time	$t_{OFF_MIN_BL}$	Sample rate = 24MHz	183.3	--	--	ns
		Sample rate = 4MHz	1100	--	--	
		Sample rate = 1MHz	5500	--	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn on Delay from PWM = 0 to PWM = 50% Duty Cycle	$t_{START_UP_BL}$	24MHz sample rate, FPWM = 10kHz	--	6	9	ms
PWM Shutdown Period	$t_{PWM_STBY_BL}$	Sample rate = 24MHz	0.54	0.60	0.66	ms
		Sample rate = 4MHz	0.27	3	3.3	
		Sample rate = 1MHz	22.5	25	27.5	
Pull-Down Resistance on PWM	R_{L_BLPWM}	Pull-down resistance on PWM	--	335	--	kΩ
Pull-Down Resistance on BL_EN	R_{L_BLEN}		--	388	--	kΩ
PWM Input Resolution	R_{ESPWM_BL}	50Hz < FPWM < 11kHz	--	--	11	bits
Display Bias						
Positive Voltage Accuracy	$V_{POSV_ACC_DB}$	REG0XB3[5:0] = 6'b011100, I_{OUT} = 0mA	-1	--	1	%
Negative Voltage Accuracy	$V_{NEGV_ACC_DB}$	REG0XB4[5:0] = 6'b011100, I_{OUT} = 0mA	-1.5	--	1.5	%
POS Ripple	V_{RIPPLE_POS}	REG0xB2[5:0] = 0'b100010, REG0XB3[5:0] = 0'b011110, I_{OUT} = 0mA	--	20	--	mV
NEG Ripple	V_{RIPPLE_NEG}	REG0xB2[5:0] = 0'b100010, REG0xB4[5:0] = 0'b011110, I_{OUT} = 0mA	--	75	--	mV
Display Bias LDO Dropout Voltage	V_{DROP_DB}	V_{DB_BST} = V_{DB_POS} = 5.2V, I_{OUT} = 80mA	--	35	70	mV
BST Switching Frequency	f_{SW_DB}		0.9	1.0	1.1	MHz
Maximum Duty Cycle	D_{MAX_DB}		90	91	--	%
BST N-MOSFET On-Resistance	$R_{ON_N_DB}$		0.05	0.3	0.6	Ω
BST P-MOSFET On-Resistance	$R_{ON_P_DB}$	REG0XB2[5:0] = 6'b100010	0.05	0.5	1	Ω
Charge Pump Equivalent Resistance	$R_{EQ_CP_DB}$	$V_{DB_BSTVOUT}$ = 5.2V, I_{NEG} = 50mA	--	2.4	--	Ω
POS Discharge Resistor	R_{DISCHP_DB}	REG0xB1[5] = 1'b1	--	70	--	Ω
NEG Discharge Resistor	R_{DISCHN_DB}	REG0xB1[2] = 1'b1	--	20	--	Ω
BST Current Limit	I_{BSTOCP_DB}	REG0xB2[5:0] = 6'b100010	0.88	1.1	1.32	A
POS Short-Circuit Protection Voltage	V_{SCPP_DB}		--	0.8 x DB_VPOS	--	V
NEG Short-Circuit Protection Voltage	V_{SCPN_DB}		--	0.25 - 0.8 x DB_VNEG	--	V
Pull-Down Resistance on DB_ENN	$R_{L_DB_ENN}$		--	386	--	kΩ
Pull-Down Resistance on DB_ENP	$R_{L_DB_ENP}$		--	386	--	kΩ
USB_PD						
Bit Rate	$f_{BitRate_PD}$		270	300	330	Kbps

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum difference between the bit rate during the part of the packet following the Preamble and the reference bit-rate.	$p_{BitRate_PD}$		--	--	0.25	%
Time from the end of last bit of a frame until the start of the first bit of the next Preamble.	$t_{InterFrameGap_PD}$		25	--	--	µs
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line	$t_{StartDrive_PD}$		-1	--	1	µs
Time to cease driving the line after the end of the last bit of the frame.	$t_{EndDriveBMC_PD}$		--	--	23	µs
Fall Time	t_{Fall_PD}		300	--	--	ns
Time to cease driving the line after the final high-to-low transition	$t_{HoldLowBMC_PD}$		1	--	--	µs
Rise Time	t_{Rise_PD}		300	--	--	ns
Voltage Swing	V_{Swing_PD}		1.05	1.125	1.2	V
Transmitter Output Impedance	z_{Driver_PD}		33	--	75	Ω
Time window for detecting non-idle	$t_{TransitionWindow_PD}$		12	--	20	µs
Receiver Input Impedance	z_{BmcRx_PD}		1	--	--	MΩ
Operating Supply Current	I_{OP_PD}	Cable attached (Full function on)	--	2.8	--	mA
Idle Mode Current (Act as a source)	$I_{IDLE_SRC1_PD}$	Cable attached with Ra, Rd	--	300	--	µA
Idle Mode Current (Act as a source)	$I_{IDLE_SRC2_PD}$	Cable attached with either Ra or Rd	--	200	--	µA
Idle Mode Current (Act as a sink)	$I_{IDLE_SNK_PD}$	Cable attached	--	125	--	µA
Low-Power Mode	$I_{LOW\text{-}POWER_PD}$	Cable unattached, $V_{PD_VCONN5V}$ = 5V	--	20	--	µA
		Cable unattached, $V_{PD_VCONN5V}$ = 0V	--	10	--	
Shipping-Mode Current	I_{SHIP_PD}		--	1	--	µA
VCONN Switch On-Resistance	$R_{ON_VCONN_PD}$		--	0.7	1	Ω
OCP Range	I_{OCP_PD}		200	--	600	mA
Time for VCONN Switch to Turn-On State	$t_{D_SOFT_PD}$		--	1.2	--	ms
DFP 80µA CC Current	$I_{CC_DFP80\mu_PD}$		64	80	96	µA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DFP 180μA CC Current	$I_{CC_DFP180\mu_PD}$		166	180	194	μA
DFP 330μA CC Current	$I_{CC_DFP330\mu_PD}$		304	330	356	μA
UFP Pull-Down Resistance through CC Pin	$Rd_{_PD}$		4.59	5.1	5.61	kΩ
UFP Pull-Down Threshold Voltage in Dead Battery	$V_{TH_DBL_PD}$	Under I_{CHG} = $I_{CC_DFP80\mu_PD}$ and $I_{CC_DFP180\mu_PD}$	0.2	--	1.6	V
UFP Pull-Down Threshold Voltage in Dead Battery	$V_{TH_DBH_PD}$	Under I_{CHG} = $I_{CC_DFP330\mu_PD}$	0.8	--	2.45	V
Valid VBUS Detection Threshold	$V_{VALID_VBUS_PD}$		3.5	--	4.0	V
RGB LED Driver						
Current Accuracy	$I_{LED_ACC_RGB}$	I_{LED} = 20mA	-4	--	4	%
Current Matching	$I_{LED_MATCH_RGB}$	I_{LED} = 20mA	-3	--	3	%
Dropout Voltage	V_{DROP_RGB}	I_{LED} = 20mA	--	200	300	mV
LED Open-Circuit Protection Threshold	$V_{TH_OPP_RGB}$	Any ISINK voltage lower than open LED protection threshold	40	100	160	mV
LED Short-Circuit Protection Threshold	$V_{TH_SCP_RGB}$	Any ISINK voltage higher than short LED protection threshold	VSYS - 0.88	VSYS - 0.5	VSYS - 0.12	V
LDO						
Input Voltage Range	V_{IN_LDO}		2.7	--	5	V
Output Voltage Range	V_{OUT_LDO}		1.6	--	4	V
Output Voltage Accuracy	ΔV_{OUT_LDO}	V_{IN_LDO} = (V_{OUT_LDO} + V_{DROP}) to 5V, I_{OUT} = 0mA to 400mA	-3	--	3	%/V
Load Current	I_{LOAD_LDO}	V_{IN_LDO} = (V_{OUT_LDO} + V_{DROP}) to 5V	0	--	400	mA
Output Current Limit	I_{LIM_LDO}	V_{IN_LDO} = (V_{OUT_LDO} + V_{DROP}) to 5V, V_{OUT} = 70% of V_{OUT} (Target)	500	--	--	mA
Dropout Voltage	V_{DROP_LDO}	V_{IN_LDO} > 2V, I_{OUT} = 0.3A	--	--	180	mV
Load Regulation	ΔI_{LOAD_LDO}	V_{IN_LDO} = (V_{OUT_LDO} + V_{DROP}) to 5V, I_{OUT} = 1mA to 400mA	-0.2	0.06	0.2	%/mA
Line Regulation	ΔV_{LINE_LDO}	V_{IN_LDO} = (V_{OUT_LDO} + V_{DROP}) to 5V, I_{OUT} = 1mA to 400mA	-1	0.5	1	%/V
Power Supply Rejection Ratio	$PSRR_{LDO}$	V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 2.8V, IOUT = 20mA @ 1kHz, LDO_COUT = 2.2μF (Note7)	--	50	--	dB
Inrush Current	I_{INRUSH_LDO}	I_{OUT} = 0mA, LDO_COUT = 2.2μF (Note7)	--	--	500	mA
Soft-Start Time	t_{SS_LDO}	I²C Enable to V_{OUT_LDO} = 90% of V_{OUT_LDO} (Target), LDO_COUT = 2.2μF @ Forced turn-on BASE (REG0x10[1] = 1'b1) (Note7)	--	--	300	μs
Discharge Time	t_{DISCHG_LDO}	I²C Disable to V_{OUT_LDO} = 10% of V_{OUT_LDO} (Target), LDO_COUT = 2.2μF (Note7)	--	--	500	μs
I²C Characteristics						
LOW-Level Input Voltage	$V_{IL_I^2C}$		--	--	0.4	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HIGH-Level Input Voltage	$V_{IH_I^2C}$		1.2	--	--	V
LOW-Level Output Voltage	$V_{OL_I^2C}$	Open-drain	--	--	0.4	V
Input Current Each IO Pin	$I_{IN_I^2C}$	0.1 x V_{DD} < V_I < 0.9 x $V_{DD(MAX)}$	-10	--	10	µA
SCL Clock Frequency	$f_{SCL_I^2C_HSM}$	CB ≤ 100pF	--	--	3.4	MHz
		100pF ≤ CB ≤ 400pF	--	--	1.7	
Data Hold Time	$t_{DH_I^2C}$		30	--	--	ns
Data Set-Up Time	$t_{DS_I^2C}$		70	--	--	ns

Note 5: A 10kΩ NTC thermistor with β = 3435K is suggested, and a SEMITEC 103KT1608T is in use.

Note 6: Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

Note 7: Guarantee by design.

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3 Application Information

3.1 General Descriptions

The MT6371 is a highly-integrated smart power management IC, which includes a single-cell Li-ion/Li-polymer switching battery charger, a USB Type-C PD controller, dual Flash LED current sources, a RGB LED driver, Backlight WLED driver, a display bias driver and a general LDO for portable devices.

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3.2 VDDA Under-Voltage Protection and Over-Voltage Protection

The device provides VDDA under-voltage protection (VDDA UVP) and over-voltage protection (VDDA OVP). If V_{DDA} falls below V_{VDDA_UVLO} or if V_{DDA} exceeds V_{VDDA_OVP}, VDDA UVP or VDDA OVP will be triggered, respectively, and the channels which will be turned off can be selected by (0x0E, bit[7:0]).

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3.3 Over-Temperature Protection

The MT6371 also features over-temperature protection (OTP), which can be triggered to shut down the device if the junction temperature exceeds T_{OTP}, 160°C typically. The channels which will be turned off can be selected by (0x0F, bit[7:4]).

If the junction temperature drops by a hysteresis of T_{OTP_HYS}, 20°C typically, the device can be reactivated.

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3.4 MRSTB Pin

The device provides a MRSTB pin to manually reset the hardware or registers.

This function is enabled by 0x01 bit [4] = 1. The debounce time can be selected by 0x01 bit [3:1], and the reset method can be selected by 0x01 [0]. The control diagram is shown in the following.

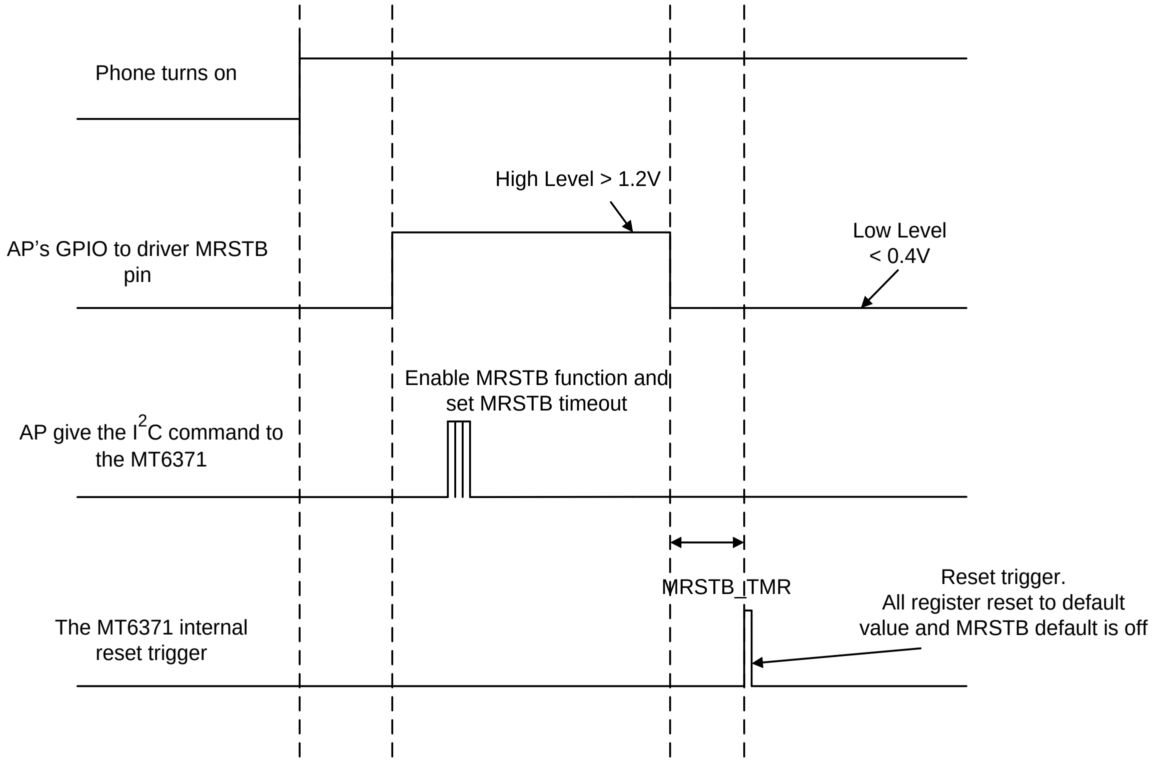

Figure 3-1. MRSTB function

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3.5 Switching Charger

The switching charger integrates a synchronous PWM controller with power MOSFETs to provide Minimum Input Voltage Regulation (MIVR), Average Input Current Regulation (AICR), high-accuracy current and voltage regulation, and charge termination. The charger also features OTG (On-The-Go) boost mode.

The switching charger has three operation modes: charge mode, boost mode (OTG-Boost), and high-impedance mode. In charge mode, the charger supports a precision charging system for single-cell batteries. In boost mode, the charger works as a boost converter to boost the battery voltage back to the CHG_VIN pin for sourcing OTG devices. In high-impedance mode, the charger stops charging or boosting and operates at a low sinking current from the CHG_VIN pin or the battery to reduce power consumption when the device is in standby mode.

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3.6 Charger Mode Operation

3.6.1 Minimum Input Voltage Regulation (MIVR)

The switching charger features Minimum Input Voltage Regulation function to prevent input voltage drop due to insufficient current provided by the adapter or USB input. If MIVR function is enabled, the input voltage decreases when the over current of the input power source occurs. VBUS is regulated at a predetermined voltage level which can be set from 3.9V to 13.4V in 0.1V steps via I2C interface. At this time, the current drawn by the switching charger equals the maximum current value that the input power can provide at the predetermined voltage level, instead of the set value.

3.6.2 Charge Profile

The switching charger provides a precision Li-ion or Li-polymer charging solution for single-cell applications. Input current limit, charge current, end-of-current current, charge voltage, and input voltage MIVR are all programmable via the I2C interface. In charge mode, the switching charger has five regulation loops to control charge current: input current, charge current, charge voltage, input voltage MIVR and device junction temperature. While charging a battery, all five loops (if MIVR is enabled) are enabled, but only one of them will dominate the charging behavior at a time.

For normal charging operation, the switching charger starts from pre-charge mode. When the battery voltage rises above a pre-charge threshold voltage (VPRECHG_CHG), the charger enters fast-charge mode. Once the battery voltage approaches the regulation voltage (VOREG_CHG), the charger enters constant voltage mode.

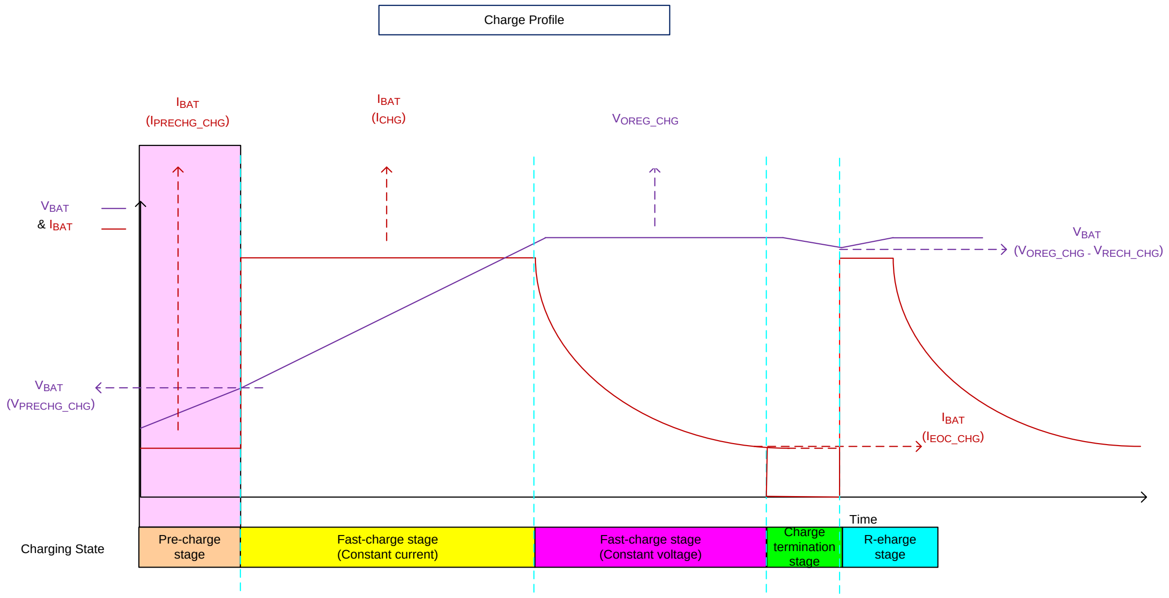

Figure 3-2. Pre-charge mode

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3.6.3 Pre-Charge Mode

To prolong battery life, the battery under low battery condition cannot be charged with a large current. When the VBAT pin voltage is below pre-charge threshold voltage (VPRECHG_CHG), the charger is in pre-charge mode and provides a weak charge current equal to a pre-charge current (IPRECHG_CHG).

There are two control loops in pre-charge mode. One is the ICHG and the other is the SYSREG. If the battery voltage is lower than the VSYS voltage, the BATFET will not be fully turn-on so that the VSYS is not equal to VBAT. That is, the VSYS can be powered by the buck converter rather than the low battery, which is being charged by the pre-charge current. As a result, the system power can be guaranteed in such low battery condition.

The pre-charge current levels IPREC (0x18, bit[3:0]) are programmable from 100mA to 850mA in a step of 50mA via the I2C interface.

3.6.4 Fast-Charge Mode and Settings

Once the VBAT pin rises above VPRECHG_CHG, the charger enters fast-charge mode and starts fast charging. Notice that a MUIC integrates input power source detection function, from an AC adapter or USB input, and the switching charger can automatically set the charge current with options accordingly. Different from a linear charger (LDO-based), the switching charger (buck-based) is like a current amplifier because the current sinking to the switching charger is different from the current sourcing into the battery.

Average Input Current Regulation (AICR) levels (0x13, bit[7:2]) and output charge current (ICHG) (0x17, bit[7:2]) are all user-programmable.

3.6.5 Cycle-by-Cycle Current Limit

The switching charger features an embedded cycle-by- cycle current limit for output inductor. Once the inductor current reaches the current limit, the charger stops charging immediately to prevent the device from being damaged by the over-current condition. Note the protection can be disabled in no case.

3.6.6 Average Input Current Regulation (AICR)

The AICR current setting is programmed via the I2C interface. For example, AICR 100mA Mode limits the input current to 100mA, and AICR 500mA Mode to 500mA. If not needed, this function can be disabled. The AICR current levels are in the range of 100mA to 3250mA with a resolution of 50mA.

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3.6.7 Average Input Current Level (AICL)

The AICL levels can be set via the I2C interface (0x1E[7:0]). When IAICR is set to large current and the VBUS voltage drops to the VMIVR level, AICL measurement mechanism will decrease IAICR level step by step automatically until the VBUS voltage exceeds AICL threshold voltage.

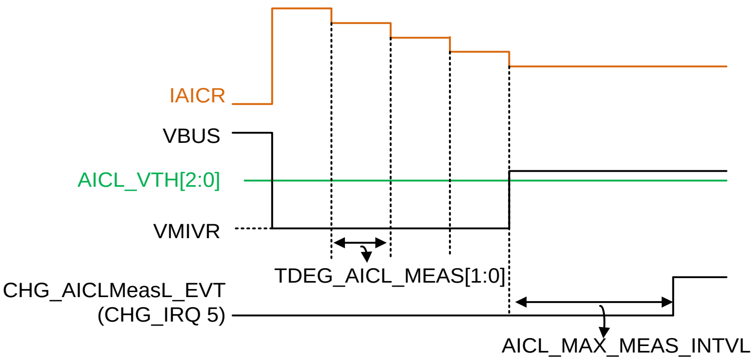

Figure 3-3. Average input current level

3.6.8 Charge Current (I_{CHG})

The charge current into the battery is determined by the sensed power path on-resistance and I²C-programmable ICHG setting. The voltage between the VSYS and VBAT pins is regulated to the voltage controlled by the ICHG setting, and the fast-charge currents (I_{CHG}) are I²C programmable from 500mA to 5000mA with a resolution of 100mA.

3.6.9 Constant Voltage Mode

The switching charger enters constant voltage mode when the VBAT voltage approaches the output regulation voltage (V_{OREG_CHG}). When entering this mode, the charge current (I_{BAT}) will begin to decrease. For default settings (charge current termination (IEOC) function is disabled), the charger will not be turned off and will always regulate the battery voltage at V_{OREG_CHG}. However, if charge current termination (IEOC) function is enabled, the charger will be turned off or battery charging is terminated when the charge current is below an end-of-charge current (I_{EOC_CHG}) in constant-voltage mode. The output regulation voltage is I²C programmable from 3.9V to 4.71V in 10mV steps.

3.6.10 End-of-Charge Current (I_{EOC_CHG})

If the charge current termination (IEOC) is enabled, the end-of-charge current is determined by the termination current sense voltage (V_{EOC}). I_{EOC_CHG} can be set via the I2C interface from 100mA to 850mA in 50mA steps.

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When input power source is plugged in, the MT6371 checks the current sourcing capability of the input power source when V_{BUS} exceeds 3.3V. The following conditions should be met to start battery charging.

1. CHG_VIN is below 14.5V (CHG_VIN OVP).
2. V_{CHG_VIN} is above 3.8V ($V_{BAD_ADP_CHG}$) when sinking 50mA ($I_{BAD_ADP_SINK_CHG}$) during 30ms of bad adapter detection time, $t_{BAD_ADP_DET_CHG}$. And this detection function can be disabled by setting ADP_DIS (0x1B, bit[7]) register bit = 1.

The charge modes as below, and the charge mode which the charger operates in will be determined according to the V_{BAT} level:

	Battery Voltage Level V_{BAT}	Battery Charge Current I_{BAT}
Trickle Mode	V_{BAT} < 2V	100mA
Pre-charge Mode	V_{BAT} < VPREC (0x08, bit[7:4])	IPREC (0x08, bit[3:0])
Fast-charge Mode	V_{BAT} < VOREG (0x04, bit[7:1])	Charge current is determined by several control loops
End-of-charge Mode	V_{BAT} = VOREG (0x04, bit[7:1])	Charge current decreases naturally

In fast-charge mode, the input current limit IIN_LIM can be selected by IINLMTSEL (0x12, bit[3:2]). This flexible setting is suitable for wide applications of adapters:

1) If IINLMTSEL = 00, the input current limit IIN_LIM is decided by the lower one of IAICR = 3.25A and the current limit is set by the CHG_ILIM pin.
2) If IINLMTSEL = 01, the input current limit IIN_LIM is decided by the lower one of CHG_TYP results and the current limit is set by the CHG_ILIM pin.
3) If IINLMTSEL = 10, the input current limit IIN_LIM is decided by the lower one of IAICR register value and the current limit is set by the CHG_ILIM pin.
4) If IINLMTSEL = 11, the input current limit IIN_LIM is decided by the lower one of IAICR = 3.25A, CHG_TYP, IAICR register value and the current limit is set by the CHG_ILIM pin.

There are 2 register bits related to the CHG_VLX switching of the MT6371:

1. SEL_SWFREQ (0x11, bit[7]) :
   - If SEL_SWFREQ is disabled (set to 0), the switching frequency is 1.5MHz (default).
   - If SEL_SWFREQ is enabled (set to 1), the switching frequency is 0.75MHz.
2. FIXFREQ (0x11, bit[6]) :
   - If FIXFREQ is disabled (set to 0), the charge switching frequency would be varied when VBUS is closed to VBAT.
   - If FIXFREQ is enabled (set to 1), the charger switching frequency is fixed.

There are 3 charger-related enable bits:

1. CFO_EN (0x12, bit[1]): The CFO_EN bit is used to enable or disable charge mode and boost mode of the charger.

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2. CHG_EN (0x12, bit[0]): When the CHG_EN bit is disabled, the power path BATFET will be turned off so that the no charge current will go into the battery. That is, the input power source continuously delivers power to the system but does not charge the battery. However, if the system load is higher than the input source current limit, the power path BATFET will be immediately turned back on so that the battery power can help supply the system. The CHG_EN bit function is the same as that of the CHG_ENB pin.
3. HZ (0x11, bit[2]): When the HZ bit is enabled, most of the internal circuits of the charger will be turned off to reduce quiescent current.

In end-of-charge mode, if EOC_EN (0x19, bit[3]) is enabled, once the charge current is lower than IEOC (0x19, bit[7:4]) level and within CHG_TEDG_EOC (0x19, bit[2:0]), the PMIC will send out IRQB and CHG_IEOCI = 1 (0xC4, bit[7]). Then, the PMIC will start to check statuses of the following three bits.

1. TE (0x12, bit[4]): If this bit is enabled, the power path will be turned off, and the buck of the charger will keep providing power to the system.
2. EOC_TIMER (0x17, bit[1:0]): With CHG_IEOC1 = 1, the power path will not be turned off. The PMIC can keep charging the battery for 30 to 60 minutes to extend battery charging capacity.
3. BATD_EN (0x1B, bit[6]): After charge is done, the MT6371 will start to sink a sink current of $I_{BAT_SINK_CHG}$ 375μA from the battery for about 256ms. If V_{BAT} drops to trigger the recharge function, the battery is as not connected to the charger. The PMIC will continue on battery detection for every two seconds.

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3.7 OTG Mode Operation

The MT6371 also supports OTG mode. It not only provides several output current limit protection levels, but also has low battery protection for overall system considerations. The MT6371 can select switching frequency via SEL_SWFREQ (0x11, bit[7]), whether the MT6371 already operates in OTG mode or not.

There are two ways to enable OTG mode:

1. By way of software: through I²C to set OPA_MODE (0x11, bit[0]).
2. By way of hardware: through I²C to set OTG_PIN_EN (0x11, bit[1]) and OPA_MODE (0x11, bit[0]). Users can then use GPIO to change the CHG_OTG pin level to enter or exit OTG mode.

The MT6371 also provides UUG_ON (0x1D , bit1) bit, which can be applied to different applications.

1. If OTG mode and UUG_ON are enabled, the boost-mode output is on the VBUS pin, which can be used for OTG (On-the-Go) mode in mobile phones.
2. If OTG mode is enabled and UUG_ON bit is disabled, the boost-mode output is on the CHG_VMID pin, which can be used in power banks; that is, adapter power can be delivered to PD-powered devices directly.

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3.8 Shipping Mode

From a manufacturer to an end user, it may take long time for products to travel. In view of this, the MT6371 provides shipping mode to further minimize battery leakage. After enabling SHIP_MODE (0x12, bit[7]), the MT6371 will shut down internal circuits to reduce quiescent current. The delay time for BATFET to be turned off can be selected by BATDAT_DIS_DLY (0x12, bit[6]). Below list several ways to exit shipping mode.

1. Input power source is plugged in.
2. Disable SHIP_MODE bit.
3. CHG_QONB pin is pulled from Logic High to Logic Low within 1 second.
4. Enable REG_RST to reset all registers to default values.

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3.9 MeidaTek Pump Express+ (MTK, PE+)

The MT6371 can provide an input current pulse to communicate with an MTK-PE+ high voltage adapter. When EN_PUMPX is enabled, the host can increase or decrease adapter output voltage by setting PUMPX_UP_DN to the desired value. After enabling either one of them, the MT6371 will generate a VBUS current pattern for the MTK-PE+ adapter to automatically identify whether to increase or decrease output voltage (VBUS pin). Once the current pattern generation is finished, IRQB will be triggered accordingly to request the processor to read the registers.

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3.10 JEITA Protection

To enhance battery thermal protection, JEITA protection is implemented in the MT6371. JEITA guidelines were released in 2007. It includes warm and cool protection, where cool section is between T1 and T2, and warm section is between T3 and T4. See the figure below. When battery temperature is in warm section, the MT6371 will lower the charge voltage (V_{OREG_CHG}) by 200mV. If the battery is in cool section, the charger will reduce charge current by half of constant current mode current I_{CHG}. The MT6371 will stop charging the battery if the battery temperature is lower than T1 or higher than T4.

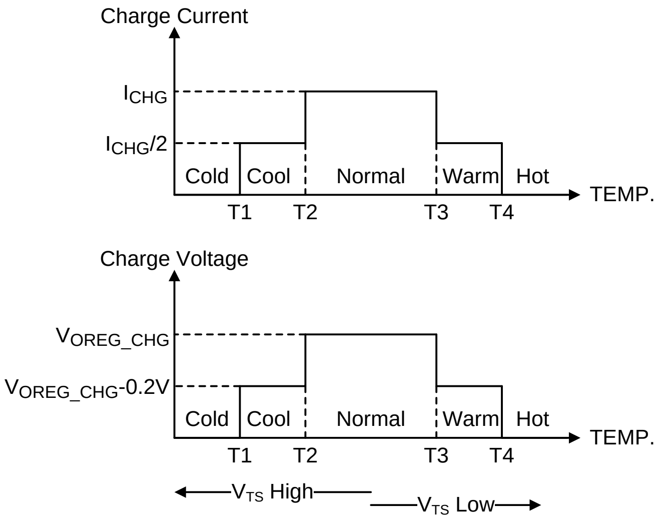

Figure 3-4. JEITA protection

The respective percentages of the voltages at T1 to T4 are shown in the following table.

No.	Parameter	Symbol	Condition	$\frac{V_{TS}}{V_{CHG_VDDP}}$	Units
1	T1 (0°C) Threshold	V_{T1}	V_{TS} rising, as percentage to V_{CHG_VDDP}	73.5	%
2	T1 Hysteresis	V_{T1_HYS}	Hysteresis, V_{TS} falling	2	%
3	T2 (10°C) Threshold	V_{T2}	V_{TS} rising, as percentage to V_{CHG_VDDP}	68.5	%
4	T2 Hysteresis	V_{T2_HYS}	Hysteresis, V_{TS} falling	2	%
5	T3 (45°C) Threshold	V_{T3}	V_{TS} falling, as percentage to V_{CHG_VDDP}	45	%
6	T3 Hysteresis	V_{T3_HYS}	Hysteresis, V_{TS} rising	2	%
7	T4 (60°C) Threshold	V_{T4}	V_{TS} falling, as percentage to V_{CHG_VDDP}	34.5	%
8	T4 Hysteresis	V_{T4_HYS}	Hysteresis, V_{TS} rising	2	%

Thermal condition of a battery can be monitored by the TS pin. There are four sections of the JEITA protection to be implemented. Based on R_{HOT} and R_{COLD}, R_{T1} and R_{T2} can be calculated with equation (1) and equation (2). Herein, R_{HOT} is the NTC resistance at the battery over-temperature threshold, and R_{COLD} is the NTC resistance at the battery under-temperature threshold.

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$R_{T1} = V_{CHG_VDDP} \times [(1/ V_{T1} - 1/ V_{T4})/(1 / R_{COLD} - 1 / R_{HOT})]$ (1)

$R_{T2} = R_{T1} \times [1 / (V_{CHG_VDDP}/ V_{T1} - R_{T1} / R_{COLD} - 1)]$ (2)

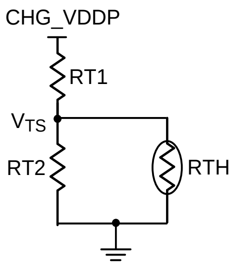

Figure 3-5. Register design for JEITA protection

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3.11 CHG_STAT Pin

There are two ways to check the MT6371's status:

By way of hardware: The MT6371's CHG_STAT pin is an open-drain output to indicate charge statuses, which are summarized in Table 3-1, for charge mode only.

Table 3-1. Charge status

Charger Status	CHG_STAT Pin Output
Charge is in progress	Low
Charge is done	High
Charge is disabled	High
Any fault occurs	Blink at 1Hz

The MT6371 status is indicated in the register 0x4A as below.

- CHG_STAT: Charger status
- BOOST_STAT: OTG boost mode status
- ADC_STAT: ADC status. Check whether ADC is active or idle

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3.12 Interrupt

The MT6371 reports status to host (CPU, MCU, EC, or etc.) by the IRQB (interrupt command to host) pin, which is an open-drain output. The IRQB pin goes low when any fault occurs. It will be automatically reset when all the fault flags are cleared.

The IRQB pin is used to indicate whether the MT6371 has any charging event. If an application processor (AP) detects a falling edge on the IRQB pin, the AP will start to read the IRQB registers 0xC0 through 0xC8 sequentially.

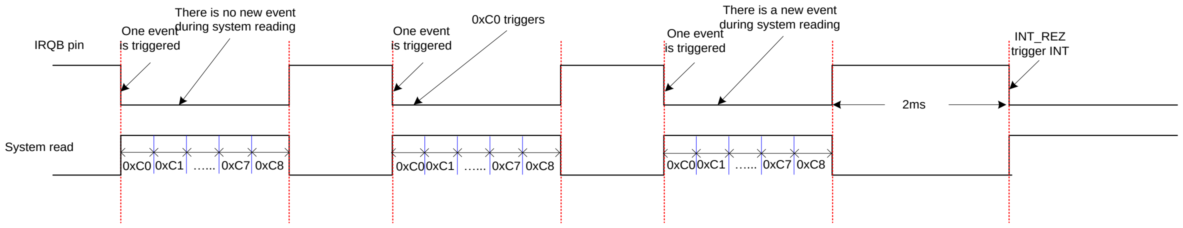

Table 3-2. IRQB pin diagram

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3.13 CHG_DSEL Pin

The CHG_DSEL pin is an open-drain output. When the device starts to detect input supply source, CHG_DSEL drives Low to indicate that detection is in progress and the device needs to take control of the D+ and D- signals. When detection is completed, CHG_DSEL holds Low if DCP (Dedicated Charging Port) or HVDCP adapter is detected. CHG_DSEL returns to High if SDP (Standard Downstream Port) or CDP (Charging Downstream Port) is detected.

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3.14 CHG_VBATOVPB Pin

Battery over-voltage protection (BAT OVP) indication is accomplished by the open-drain and active-low output, CHG_VBATOVPB: Low if BAT OVP occurs, and High, otherwise.

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3.15 Analog IR Drop Compensation

The resistance between the charger output and the battery cell terminal may cause the charger to enter constant voltage operation mode from constant current operation mode too early, and thus increase the battery charging time. To reduce the battery charging time to speed up charge cycle, the MT6371 provides IR compensation function so that the charger has more precise control over the timing that the charger operates in constant current mode, which has the maximum charge current. Host (AP) can set IR compensation function by programming the register bits BAT_COM (0x2C, bit[5:3]) and VCLAMP (0x2C, bit[2:0]). The formula is as below:

$V_{ACTUAL} = V + \min.(I_{CHG}\ (\text{Actual}) \times BAT_COM,\ V_{CLAMP})$

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3.16 ILIM Pin

For hardware protection, the MT6371 supports input current limit setting on the ILIM pin by way of a resistor from ILIM pin to ground.

$I_{INMAX} = K_{ILIM} / R_{ILIM}$

For example, if the input current limit is to be set as 2A with a typical input current limit factor KILIM as 355AΩ, a resistor of 180Ω will then be chosen as the resistor from the ILIM pin to ground. The actual input current limit is the minimum between the result of IINLMTSEL (0x12, bit[3:2]) and ILIM.

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3.17 ADC Conversion Operation Flow

The figure below shows the flow chart of ADC conversion operation. ADC conversion starts from selecting an ADC channel by setting ADC_IN_SEL (0x21, bit[7:4]) and enabling ADC_START (0x21, bit[0]). After about 200ms of ADC conversion time for a conversion to be completed, ADC_DONEI (0xC5, bit[0]) will be enabled and ADC_STAT (0x4A, bit[0]) will be disabled. The host can be informed that ADC conversion is completed by reading the register bits.

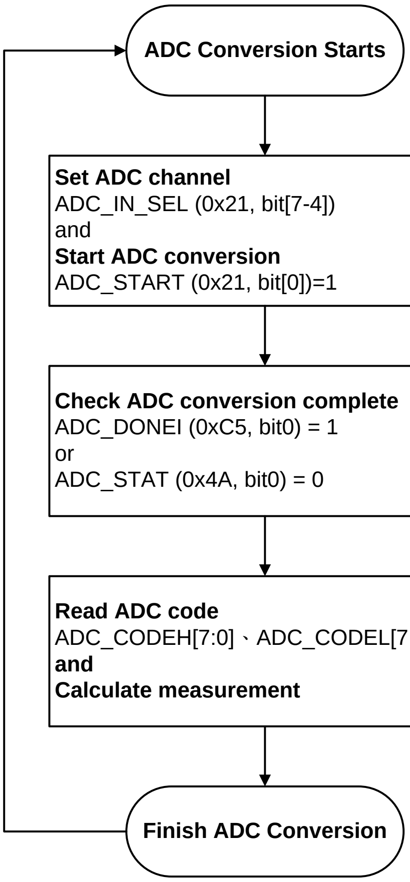

Figure 3-6. ADC conversion operation flow

The host can read ADC high-byte codes from ADC_CODEH (0x4C, bit[7:0]) and low-byte codes from ADC_CODEL (0x4D, bit[7:0]) to calculate the measured voltage/current/temperature data with respect to each ADC channel. The table below shows measurement equations for various ADC channels. When measuring IBUS, AICR setting needs large 350mA at least. When measuring IBAT, the ICHG setting needs large 1A at least.

ADC Channel	Measurement Equation	Measurement Range
VBUS_DIV5	[(ADC_CODEH x 256) + ADC_CODEL] * 25mV	1V to 22V
VBUS_DIV2	[(ADC_CODEH x 256) + ADC_CODEL] * 10mV	1V to 9.1V
VBAT	[(ADC_CODEH x 256) + ADC_CODEL] * 5mV	0V to 4.9V
VSYS	[(ADC_CODEH x 256) + ADC_CODEL] * 5mV	0V to 4.9V

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ADC Channel	Measurement Equation	Measurement Range
CHG_VDDP	[(ADC_CODEH x 256) + ADC_CODEL] * 5mV	0V to 4.9V
TS_BAT	[(ADC_CODEH x 256) + ADC_CODEL] * 0.25%	0% to 100%
IBUS IAICR[5:0] setting < 400mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA * 0.67	0A to 0.4A
IBUS IAICR[5:0] setting ≥ 400mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA	0A to 5A
IBAT ICHG[5:0] setting 500mA to 850mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA * 0.536	0A to 0.85A
IBAT ICHG[5:0] setting ≥ 900mA	[(ADC_CODEH x 256) + ADC_CODEL] * 50mA	0A to 5A
TEMP_JC	[(ADC_CODEH x 256) + ADC_CODEL] * 2°C - 40°C	-40°C to 120°C

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3.18 USB_PD

The PD function of the MT6371 complies with USB Type-C Port Controller Interface spec 1.0. Some "Not support" functions are listed in the register table.

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3.19 Type-C Detection

The USB_PD implements multiple comparators which can be used by software to determine the state of the PD_CC1, PD_CC2 pins. This status information provides the host processor all of the information required to determine attach and detach status of the cable.

The USB_PD has three threshold comparators, which match the USB Type-C specification for the three charge current levels, which can be detected by a Type-C device. These comparators can automatically trigger interrupts to occur when there is a change of state.

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3.20 Detection through Autonomous DRP Toggles

The USB_PD has the capability to do autonomous DRP toggles. In DRP toggles, the MT6371 implements DRP toggle between SRC (source) and SNK (sink). It can also present as a SRC or SNK only and monitor PD_CC1, PD_CC2 status.

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3.21 PD Protocol Communication

ype-C connectors allow USB Power Delivery (PD) to communicate over the connected PD_CCx pins between two ports. The communication method is the BMC Power Delivery protocol. Possible usages are outlined below:

- Negotiating and controlling power levels
- Alternate mode interfaces, such as Display Port
- Role swap for dual-role ports, switchable between as the source or sink
- Communication with USB Type-C full featured cables

The USB_PD integrates a BMC PD block, which includes a BMC physical layer and packet buffer, which allow packets to be sent and received by host software through I²C. The USB_PD allows host software to implement all features of the USB BMC PD through writes and reads of the buffer and control of the USB_PD physical interface.

Table 3-3. USB PD abbreviations

Term	Description
BMC	Biphase Mark Coding
TCPC	Type-C Port Controller
TCPCI	Type-C Port Controller Interface
TCPM	Type-C Port Manager

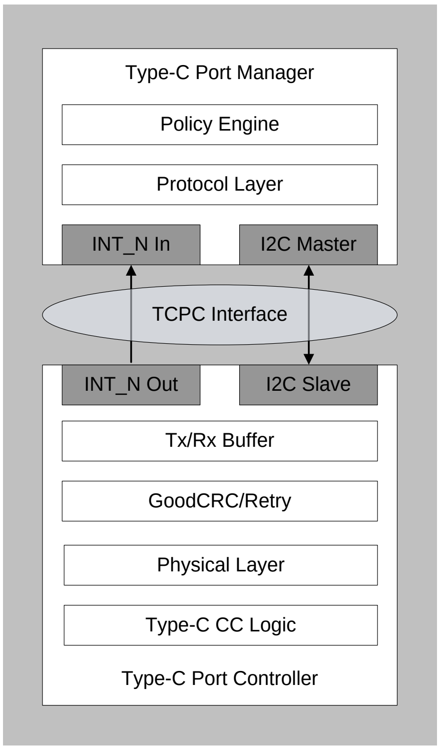

Figure 3-7. Type-C port controller (TCPC) interface

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The Type-C Port Controller Interface, TCPCI, is the interface between a Type-C Port Manager and a Type-C Port Controller.

- The Controller Interface uses the I²C protocol:
- The TCPM is the only master on this I²C bus.
- The TCPC is a slave device on this I²C bus.
- The TCPC supports Fast-Mode bus speed.
- The TCPC has an open-drain output, active-low PD_IRQB pin. This pin is used to indicate change of state, where the PD_IRQB pin is asserted when any Alert Bits are set.
- The TCPCI supports I/O nominal voltages of 1.8V and 3.3V.
- The TCPC supports auto-increment of the I²C internal register address for the last byte transferred during a read, independent of an ACK/NACK from the master.

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3.22 Display Bias

3.22.1 Output Voltage

The MT6371 provides a single high-efficiency boost converter to serve for positive and negative voltage for LCD display bias. The output voltage DB_BSTVOUT, DB_POSVOUT and DB_NEGVOUT are programmable and the operation voltage setting is shown in Table 3-4. The DB_BSTVOUT should be selected to provide enough headroom for good ripple and load transient performance. The headroom voltage between DB_BSTVOUT, and the maximum absolute value of DB_POSVOUT and DB_NEGVOUT should be higher than 200mV. The Display Bias operation can be controlled by pins or register bits with Table 3-5.

Table 3-4. Display bias operation setting

Channel	Range	Step	Register	Suggest Value
DB_BSTVOUT	4V to 6.15V	50mV/LSB	0xB2[5:0]	5.7V
DB_POSVOUT	4V to 6V	50mV/LSB	0xB3[5:0]	5.5V
DB_NEGVOUT	-4V to -6V	50mV/LSB	0xB4[5:0]	-5.5V

Table 3-5. Display bias operation control setting

DB_ext_en 0xB0[0]	DB_ENP Pin	DB_ENN Pin	DB_vpos_en 0xB1[6]	DB_vneg_en 0xB1[3]	Status
0	X	X	0	0	Standby
0	X	X	1	0	DB_POSVOUT enable
0	X	X	0	1	DB_NEGVOUT enable
0	X	X	1	1	DB_POSVOUT & DB_NEGVOUT enable
1	0	0	X	X	Standby
1	1	0	X	X	DB_POSVOUT enable
1	0	1	X	X	DB_NEGVOUT enable
1	1	1	X	X	DB_POSVOUT & DB_NEGVOUT enable

DB_ext_en 0xB0[0]	DB_ single_pin 0xB0[5]	DB_ENP Pin	DB_ENN Pin	Status
1	0	0	0	Standby
1	0	1	0	DB_POSVOUT enable
1	0	0	1	DB_NEGVOUT enable
1	0	1	1	DB_POSVOUT & DB_NEGVOUT enable
1	1	0	X	Standby
1	1	1	X	DB_POSVOUT & DB_NEGVOUT enable

3.22.2 DB_POSVOUT & DB_NEGVOUT Delay Time

The MT6371 provides a delay time control between the DB_POSVOUT and DB_NEGVOUT during power sequence. The bits of the 0xB2[7:6] are used to set the delay time. Table 3-6 and Figure 3-8 show the delay time and the sequence for Display Bias during power on and off.

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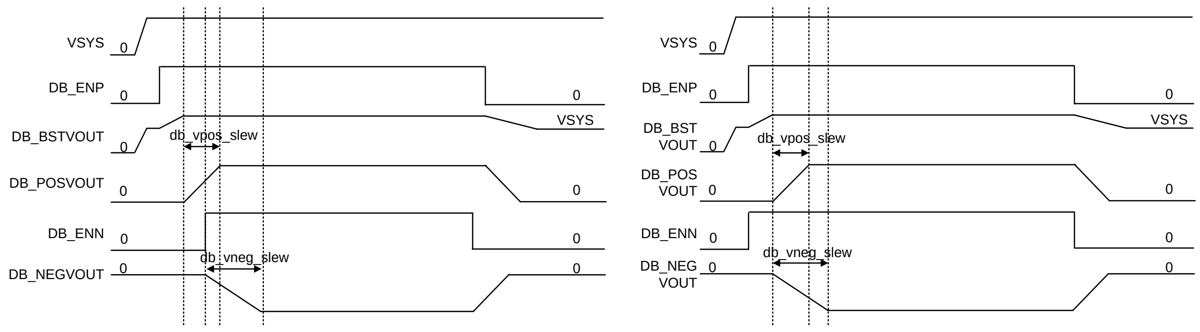
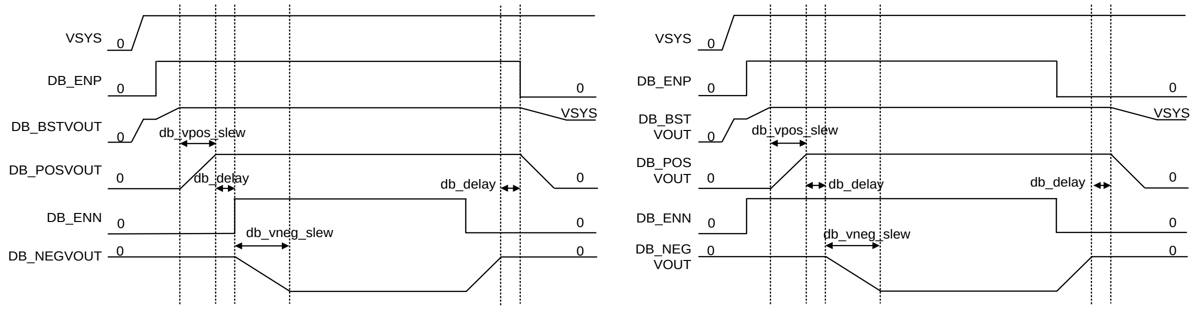
Table 3-6. Display bias delay time control setting

0xB2[7:6]	Delay Time	Power On	Power Off
00	No constraint	DB_POSVOUT start to ramp up when DB_ENP = H or db_vpos_en = 1 DB_NEGVOUT start to ramp down when DB_ENN = H or db_vneg_en = 1	DB_NEGVOUT start to discharge when DB_ENN = L or db_vneg_en = 0 DB_POSVOUT start to discharge when DB_ENP = L or db_vpos_en = 0
01	0ms	DB_POSVOUT start to ramp up when DB_ENP = H or db_vpos_en = 1 DB_NEGVOUT start to ramp down after DB_POSVOUT ramp up to target and delay 0ms even the DB_ENN = H or db_vneg_en = 1	DB_NEGVOUT start to discharge when DB_ENN = L or db_vneg_en = 0 DB_POSVOUT start to discharge after DB_NEGVOUT discharge to GND and delay 0ms even the DB_ENP = L or db_vpos_en = 0
10	1ms	DB_POSVOUT start to ramp up when DB_ENP = H or db_vpos_en = 1 DB_NEGVOUT start to ramp down after DB_POSVOUT ramp up to target and delay 1ms even the DB_ENN = H or db_vneg_en = 1	DB_NEGVOUT start to discharge to GND when DB_ENN = L or db_vneg_en = 0 DB_POSVOUT start to discharge after DB_NEGVOUT discharge to GND and delay 1ms even the DB_ENP = L or db_vpos_en = 0
11	4ms	DB_POSVOUT start to ramp up when DB_ENP = H or db_vpos_en = 1 DB_NEGVOUT start to ramp down after DB_POSVOUT ramp up to target and delay 4ms even the DB_ENN = H or db_vneg_en = 1	DB_NEGVOUT start to discharge when DB_ENN = L or db_vneg_en = 0 DB_POSVOUT start to discharge after DB_NEGVOUT discharge to GND and delay 4ms even the DB_ENP = L or db_vpos_en = 0



(a) Display Bias delay no constraint



(b) Display Bias delay between DB_POSVOUT and DB_NEGVOUT

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Figure 3-8. Display bias delay time control sequence

3.23 Periodic Mode

The MT6371 supports the DB periodic mode with the enable bit 0xB0[7] and frequency select bit 0xB0[6]. In the periodic mode, the enabled channel of the DB_POSVOUT and DB_NEGVOUT will repeat on/off sequence. The timing diagram for the periodic mode control is shown in Figure 3-9.

Table 3-7. Periodic mode control setting

db_periodic_mode 0xB0[7]	db_freq_pm 0xB0[6]	ton (ms)	tperiod (ms)
0	0	X	X
0	1	X	X
1	0	2	50
1	1	1.6	30

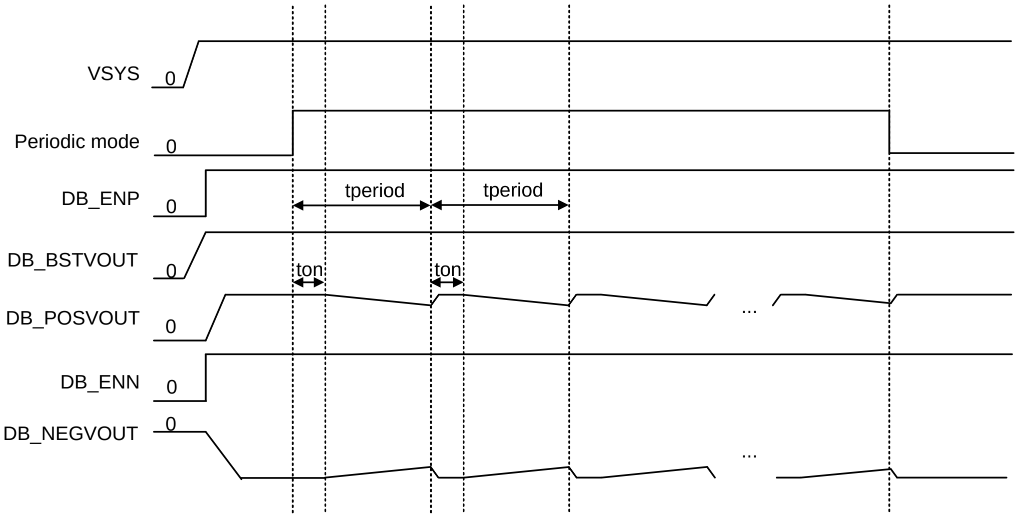

Figure 3-9. Periodic mode control

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3.24 Output Discharge and Connection to Ground

The MT6371 integrates internal switch resistors to discharge the output voltage when the channel power is off. Setting register 0xB1[4] = 1 and 0xB1[1] = 1 to enable the discharge function of DB_POSVOUT and DB_NEGVOUT individually. The output will keep connecting to GND when the register 0xB1[5] = 1 and 0xB1[2] = 1.

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3.25 FLED Flow Chart

The MT6371 provides torch mode and strobe mode operation for FLED application. Torch mode power supply by the battery directly and the strobe mode power supply by the battery operating in OTG mode. There are two power switches to select the power loop. In torch mode, the FL_VINTORCH turn on to connect to battery. In strobe mode, the CHG_VIN voltage is detected avoiding the high voltage stress to turn on the FLED. The charger will operate in OTG mode to provide the power in strobe mode.

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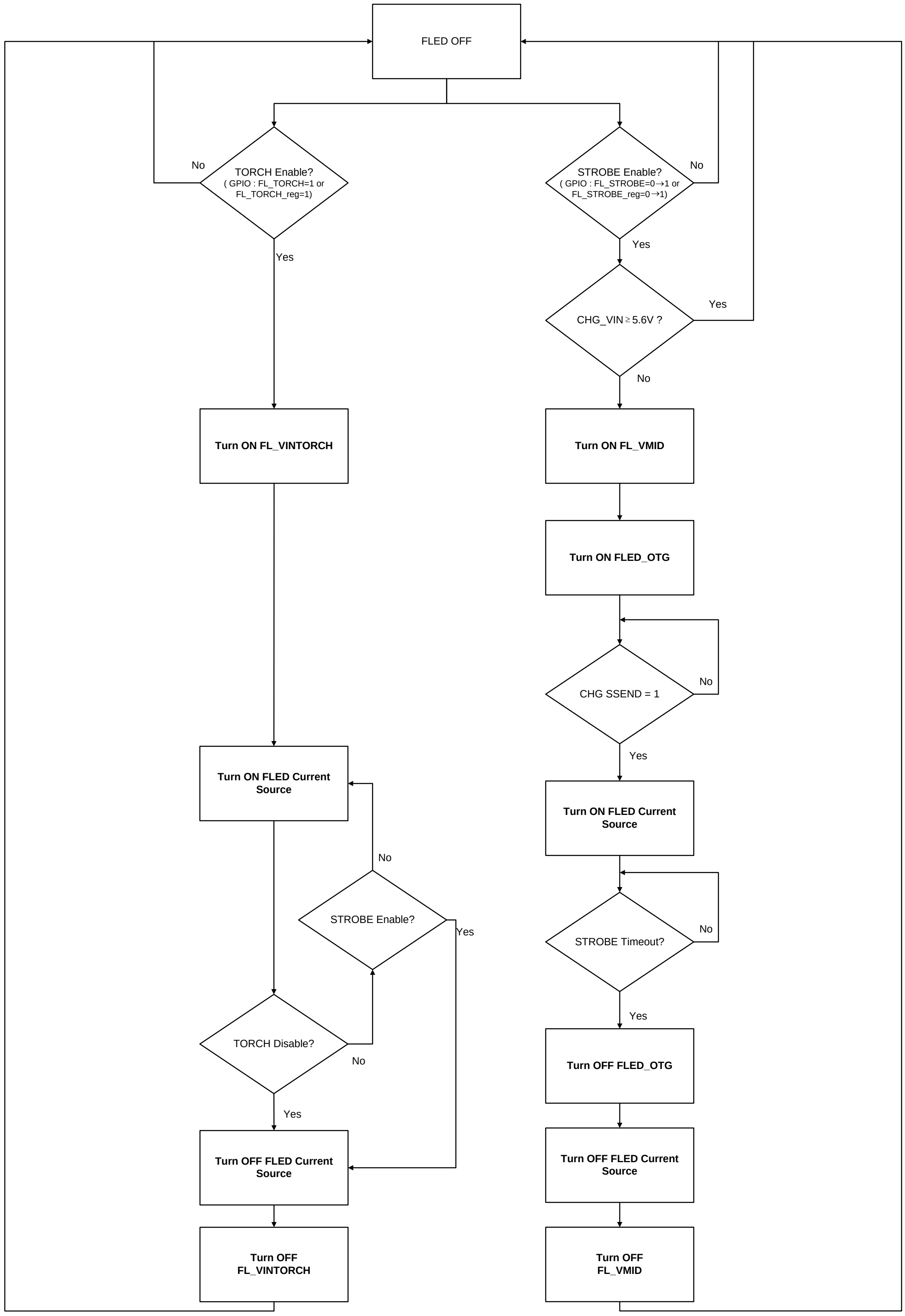

Figure 3-10. FLED flow chart

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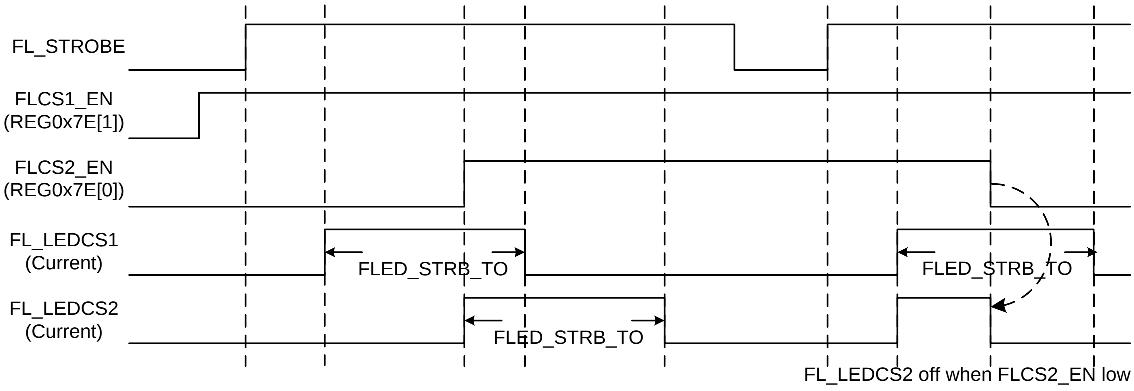
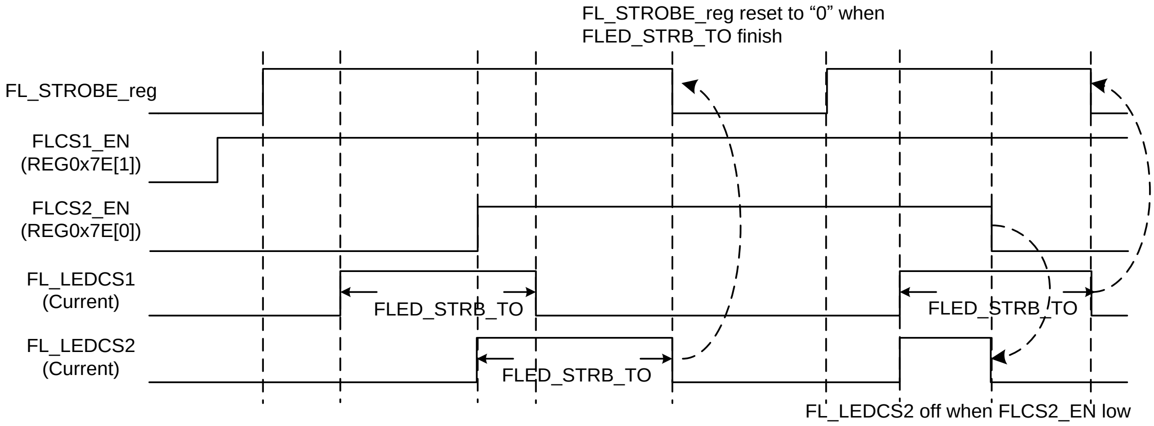
3.26 Strobe Mode Operation

The MT6371 provides 117 different current levels from 25mA to 750mA in steps of 6.25mA or 50mA to 1500mA in steps of 12.5mA in strobe mode. FLED1 and FLED2 strobe currents can be programmed by register 0x74[6:0] and register 0x78[6:0] for flash brightness. The following figure shows that when strobe target current is higher than timeout current level, it will be terminated by the strobe timeout period to elapse. FLED turns off completely after the strobe timeout which is set by register 0x73[6:0] for strobe LED1 and LED2. If the strobe target current is lower than timeout current level, it will keep lighting even the timeout is finished.



Note: If FLCS1_EN/FLCS2_EN = “0”, FLED will not be turned on even FL_STROBE enable.

Figure 3-11. FLCS1_EN and FLCS2_EN (FL_STROBE)



Note: If FLCS1_EN/FLCS2_EN = “0”, FLED will not be turned on even FL_STROBE register is set “1”.

Figure 3-12. FLCS1_EN and FLCS2_EN (FL_STROBE_reg)

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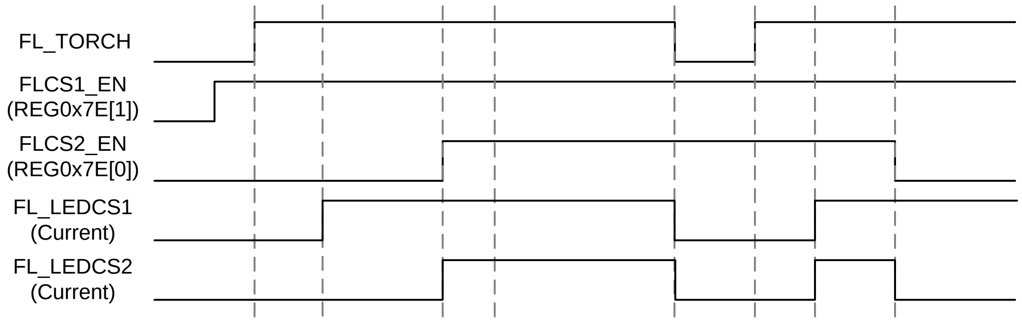
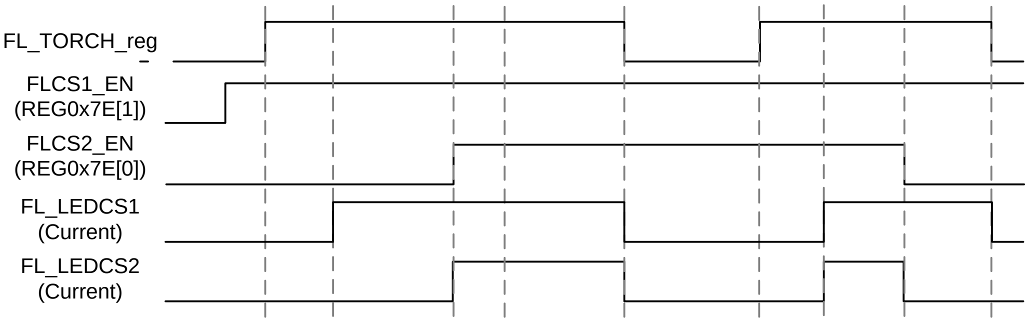
3.27 Torch Mode Operation

The MT6371 provides 31 different current levels from 25mA to 400mA in steps of 12.5mA. FLED1 and FLED2 torch currents can be programmed by reg0x75[4:0] and reg0x79[4:0] for torch brightness. Once torch mode is enabled, the current sources will ramp up to the programmed torch current.



Note: If FLCS1_EN/FLCS2_EN = "0", FLED will not be turned on even FL_TORCH enable.

Figure 3-13. FLCS1_EN and FLCS2_EN (FL_TORCH)



Note: If FLCS1_EN/FLCS2_EN = "0", FLED will not be turned on even FL_TORCH register is set "1".

Figure 3-14. FLCS1_EN and FLCS2_EN (FL_TORCH_reg)

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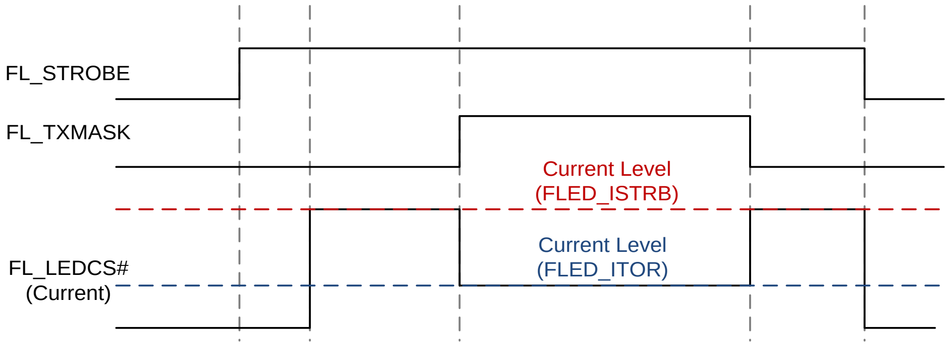
3.28 FL_TXMASK Function

The strobe current setting can be changed to torch current level setting by reg0x75[4:0] and reg0x79[4:0] when the FL_TXMASK pin goes high during strobe operation. It can release the current from torch to strobe when FL_TXMASK pin goes low within the timeout period.



Note: TXActiveLevel = 1, TXSEL<1:0> ≠ <00>

Figure 3-15. FL_TXMASK function

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3.29 FLED Short Protection

The device features a built-in protection against flash LED failures result from short-circuit. When the FL_LEDCS1 or FL_LEDCS2 voltage is lower than 1V, the current source will be clamped to 320μA to prevent the over load issue.

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3.30 Input Capacitor Selection

Input ceramic capacitor of 4.7μF is recommended for FL_VMID pin. For better voltage filtering, ceramic capacitor with low ESR is recommended. The best performance of the Flash LED can be achieved by using the capacitor of large capacitance. X5R and X7R types are suitable because of their wider voltage and temperature ranges.

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3.31 Supply Limit

When the adapter supply power is higher than $V_{OVP_STRB_FL}$ (typ. 5.6V), the flash LED will not work to protect the internal circuit.

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3.32 Low Battery Voltage Protection (LBP)

When the battery voltage is lower than a specified value, the FLED will be turned off. Until the battery voltage rises above the low battery voltage protection threshold plus hysteresis voltage value, the FLED resumes turn-on. The low battery voltage protection can be programmed with register 0x1A[7:4] for 16 different levels (2.3V to 3.8V, 0.1V step).

3.32.1 Charger adapter (CHG_VIN < VOVP_STRB_FL (typ. 5.6V)) plug in/out

If a charger power input $V_{CHG_VIN} < V_{OVP_STRB_FL}$ (typ. 5.6V) is plugged in/out, the flash LED current sources will operate the same as described before, as shown in Figure 3-16 and Figure 3-17 for torch mode and strobe mode, respectively.

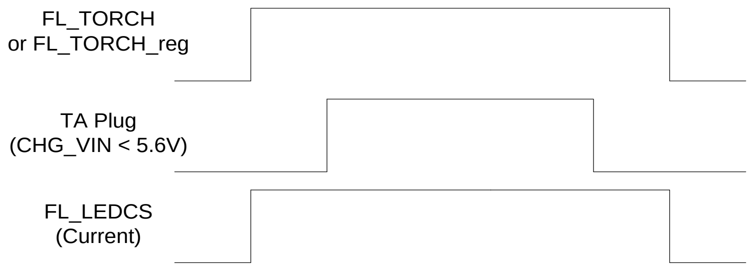

Figure 3-16. Torch case (CHG_VIN < 5.6V)

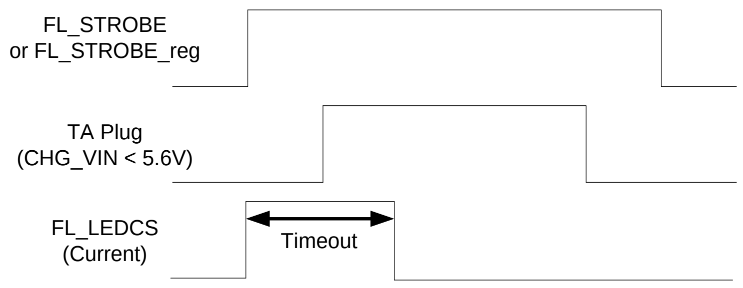

Figure 3-17. Strobe case (CHG_VIN < 5.6V)

3.32.2 Charger adapter (CHG_VIN ≥ 5.6V) plug in/out

When charger adapter (CHG_VIN ≥ 5.6V) is plugged in, there is no influence on FLED operation with torch mode and the FLED output current will be interrupted immediately with flash mode for protection.

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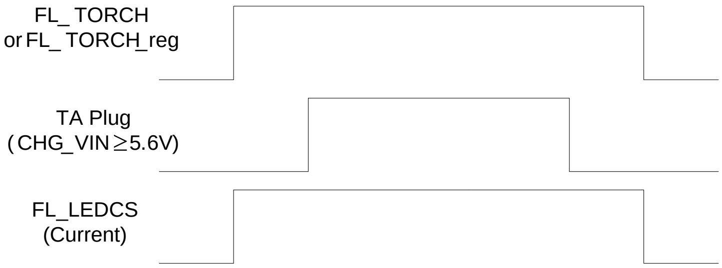

Figure 3-18. Torch case (CHG_VIN ≥ 5 .6V)

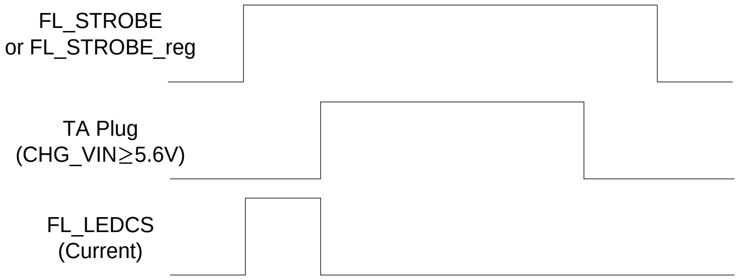

Figure 3-19. Strobe case (CHG_VIN ≥ 5.6V)

3.32.3 FLED operation with Charger in OTG mode

The CHG_VMID voltage level will change from strobe mode setting to OTG setting when the OTG function is enabled.

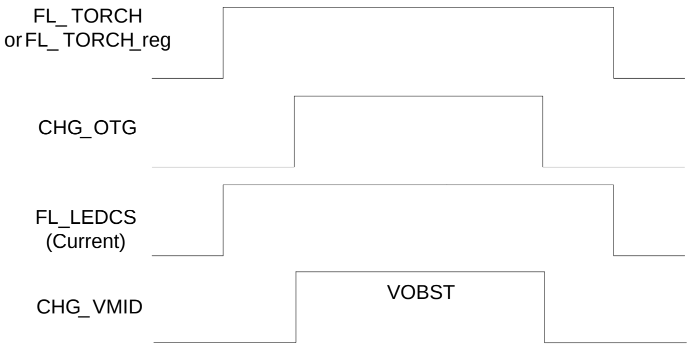

Figure 3-20. Torch case with OTG

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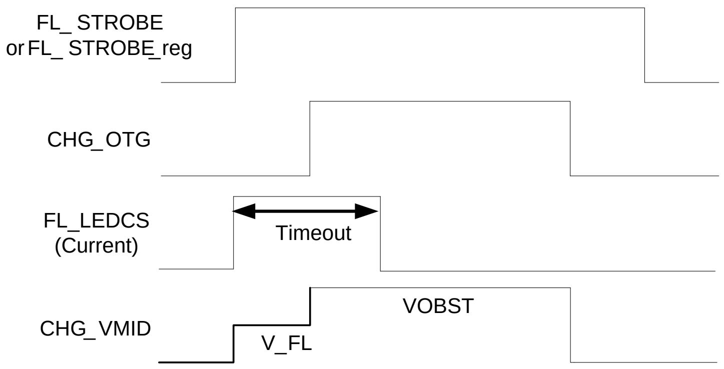

Figure 3-21. Strobe case with OTG

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3.33 RGB LED Driver

The MT6371 integrates a four-channel RGB LED driver, designed to provide a variety of lighting effects for mobile device applications. The RGB LED driver includes a smart LED string controller, and it can drive 3 channels of LEDs with a sink current of up to 24mA and a CHG_VIN power good indicator LED with a sink current of up to 6mA. It provides three operation modes for the RGB LEDs: PWM mode, breath mode, and register mode. The device can increase or decrease the brightness of the RGB LEDs upon command via the I²C interface.

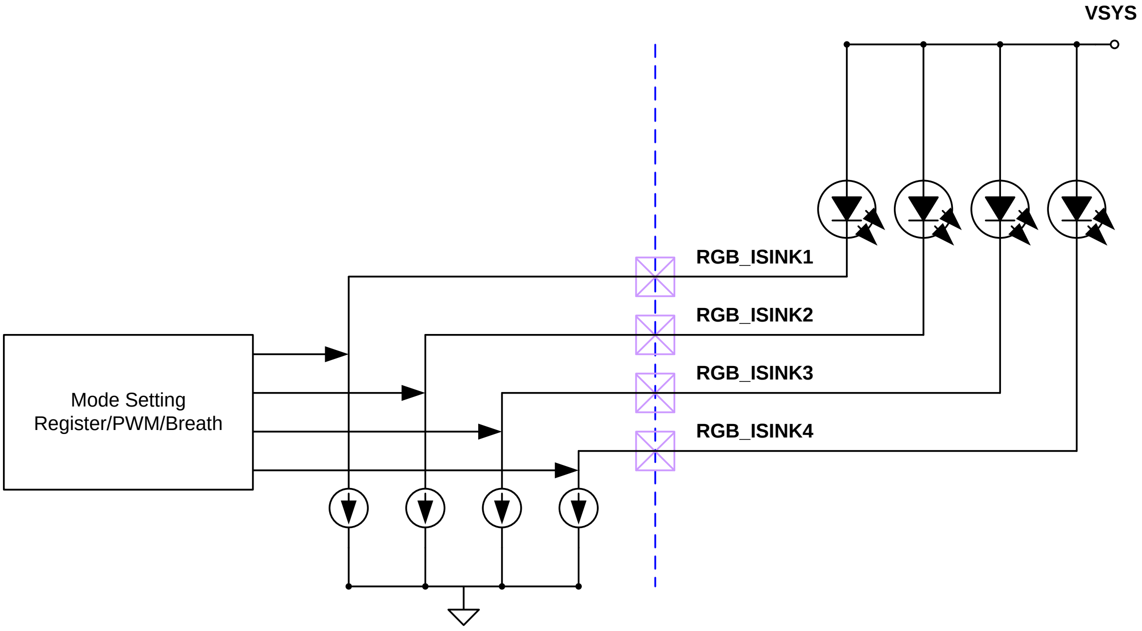

Figure 3-22. RGB LED driver application circuit

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3.34 PWM Mode

The MT6371 features a built-in PWM mode control by setting ISINKx_DIM_MODE to 00. The RGB_ISINK1 to RGB_ISINK3 of the MT6371 can provide up to 24mA per string. There are 7 step LED current control by setting ISINKx_CUR_SEL each channel. The ON/OFF of the current source is synchronized to the PWM signal. The frequency of LED current is equal to the PWM input signal that is setting by ISINKx_DIM_FSEL. In order to guarantee the PWM resolution, the PWM frequency have to be operated at range of 0.1Hz to 1kHz that is selected by ISINKx_DIM_FSEL.

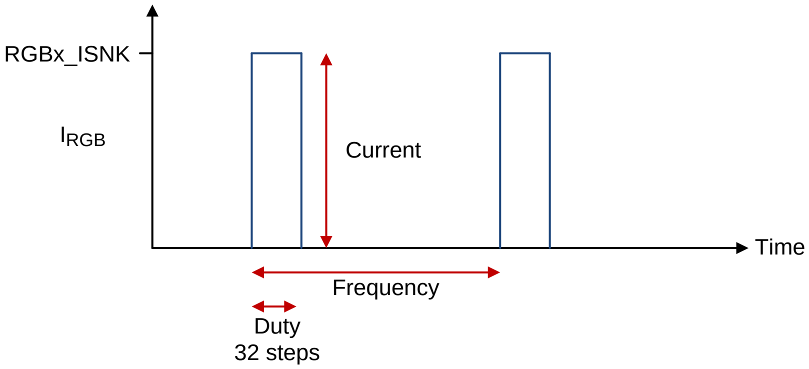

Figure 3-23. RGB PWM mode operating principle

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3.35 Breath Mode

In the breath mode, the 3 channels of the MT6371 can provide up to 24mA per string. There are 7 step LED current control by setting register ISINKx_CUR_SEL each channel.

In order to provide a smooth breath mode, there are 6 period timing to control the rising time and falling time, and it is controlled by setting register ISINKx_VREATH_TON_SEL, BISINKx_BREATH_TOFF_SEL, BISINKx_BREATH_Trx_SEL and ISINKx_BREATH_Tfx_SEL.

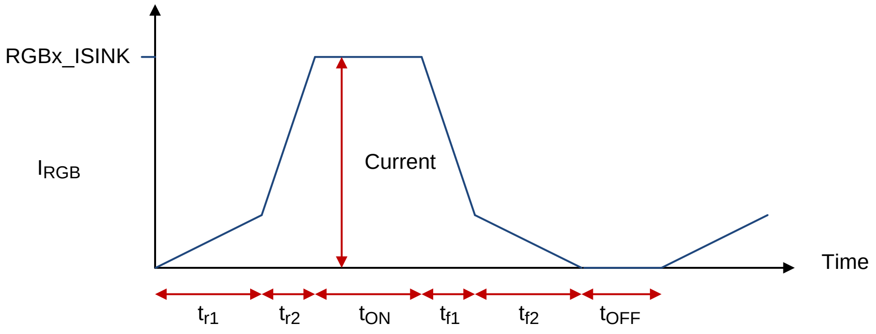

Figure 3-24. RGB breath mode operating principle

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3.36 Register Mode

The MT6371 features a built-in register mode control by setting ISINKx_DIM_MODE to 1X. The register ISINKx_SFSTR_EN controls the soft-start time ON/OFF. If ISINKx_SFSTR_EN is enable, ISINKx_SFSTRx_TC can select soft start time for the each step. The four channels of the MT6371 can provide up to 24mA per string. There are 7 step LED current control by setting register ISINKx_CUR_SEL each channel.

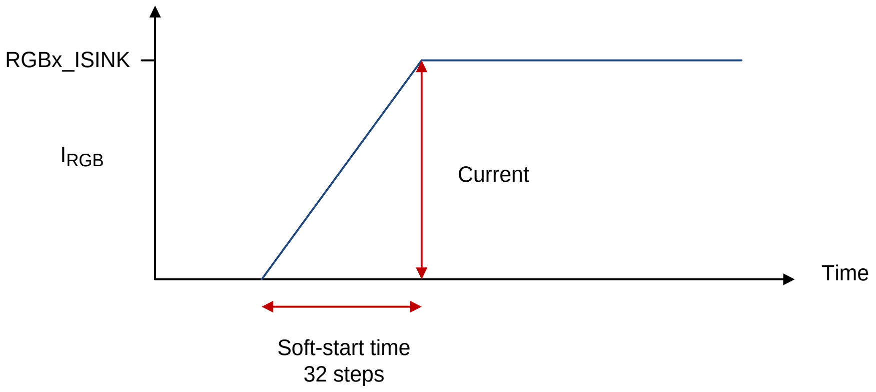

Figure 3-25. RGB register mode operating principle

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3.37 Backlight LED

The MT6371 provides brightness controllable backlight LED for 4P8S applications. The LED current level can be programmed via the register and the external BL_PWM pin. Each of the four channels can be controlled by the bits (register 0xA0[5:2]). The ramp time from a current level for one brightness level to that for another brightness level can be adjusted from 0ms to 8000ms. The MT6371 supports torch/strobe mode for backlight LED with regulated constant current. The output current provides up to 30mA for torch/strobe mode per channel white LEDs for front camera screen flash applications. A built-in programmable timer is used for strobe mode timeout function. It adopts four channels to provide accurately regulated current flow through four separate white LEDs independently. If the backlight LED is no use, it needs to disable the bled_Xch_en by setting 0xA0[5:2].

Table 3-8. BLED operation control table

BL_EN 0xA0[6]	BL_ENx 0xA0 [5:2]	BL_PWM 0xA2[7]	BL_PWM Pin	Status
0	X	X	X	Standby
1	0000	X	X	LED Bias enable
1	1111	0	X	I_{LEDx} = BLED Brightness
1	1111	1	0	LED Bias enable
1	0000	1	Duty	LED Bias enable
1	1111	1	Duty	I_{LEDx} = (BLED Brightness*PWM Duty)

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3.38 LED Brightness Current and PWM

The LED brightness current level is controlled via the register and the PWM duty cycle. LED current mapping can be set either linear or exponential. The LED current can be approximated by the equation:

Base on linear mapping, the current for the 11 bit code can be approximate by the equation:
I_{LED} = 0.0146mA x Brightness Code x PWM Duty

Base on exponential mapping, the current for the 11 bit code can be approximate by the equation:
$I_{LED} = 0.06\text{mA} \times (1.003040572203 29^{\text{Brightness Code} \times \text{PWM Duty}})$

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3.39 PWM Brightness Dimming

Besides the programmable built-in I²C backlight LED current level control, the MT6371 features a built-in PWM dimming current control by setting the register 0xA2[7] = 1, offering a linear current dimming by the external clock source. In order to guarantee the sufficient PWM dimming resolution, the dimming frequency must be operated at range of 50Hz to 50kHz.

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3.40 PWM Resolution and Input Frequency Range

The PWM input frequency range is 50Hz to 50kHz. To achieve the full 11-bit maximum resolution of PWM duty cycle to the LED brightness code, the input PWM duty cycle must be ≥ 11 bits, and the PWM sample period (1/f_{AMPLE}) must be smaller than the minimum PWM input pulse width. Figure 3-26 shows the ideal maximum resolutions based on the input PWM frequency. The minimum PWM frequency for each PWM sample rate is based on PWM timeout.

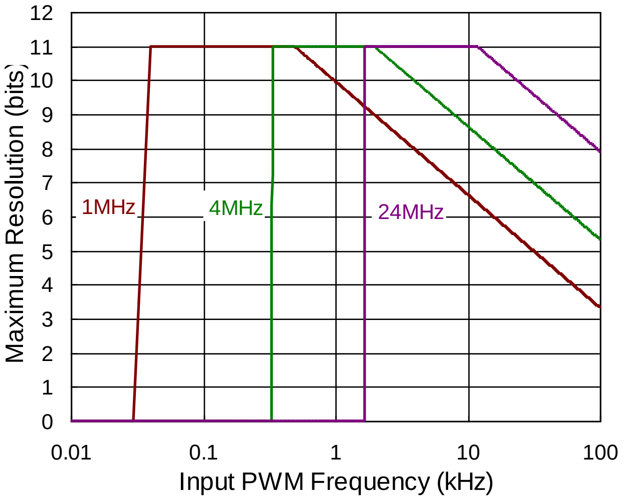

Figure 3-26. PWM sample rate, maximum resolution vs. input PWM frequency

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3.41 BLED Torch Mode

The MT6371 features a built-in BLED torch mode control with the register 0xA7[7:6] = 1X. In BLED torch mode, the MT6371 provides 256 different current levels from typically 0mA to 30mA. The torch current level for brightness is adjusted via the register 0xA9. When backlight torch mode is set, PWM control will be disabled, and backlight LED current will set to Bled_Torch_Current. The torch current, torch ramp up/down timing setting can be set by the following table.

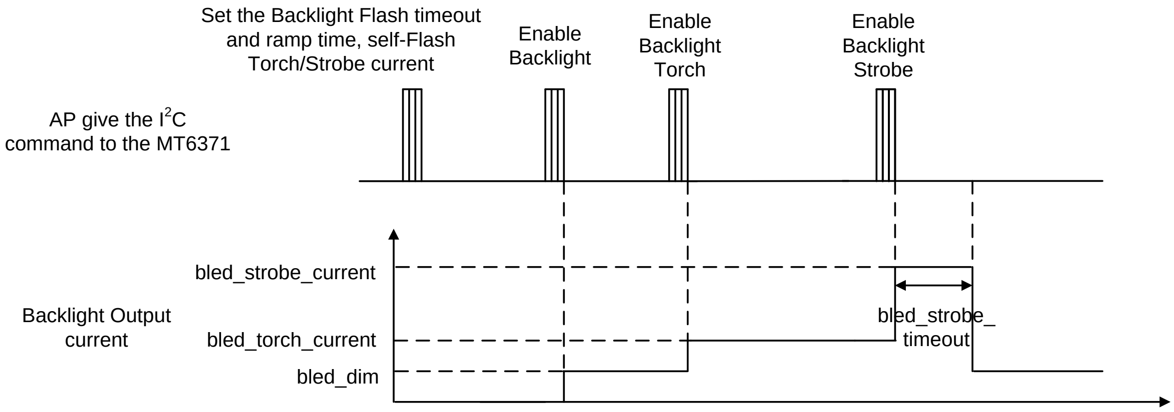

Figure 3-27. Backlight torch and strobe mode case 1

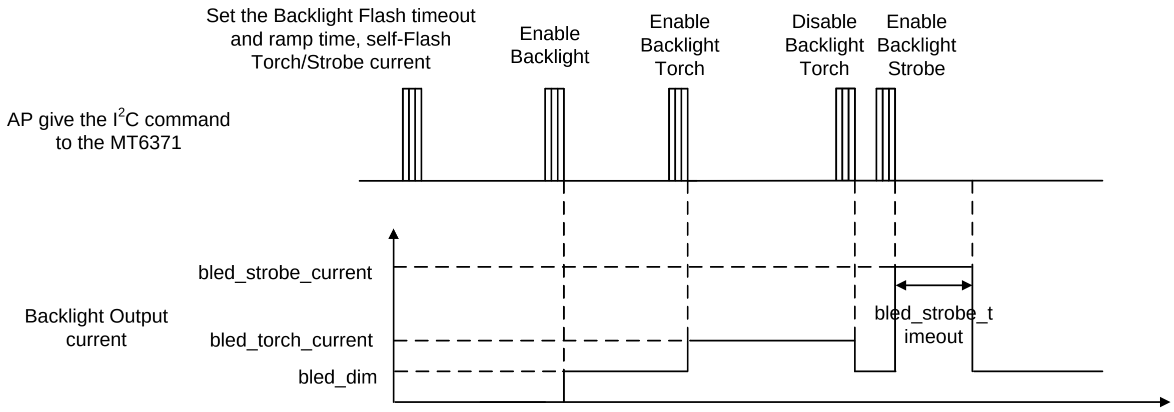

Figure 3-28. Backlight torch and strobe mode case2

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3.42 BLED Strobe Mode

The MT6371 features a built-in BLED strobe mode control with register 0xA7[7:6] = 01. In BLED strobe mode, the MT6371 provides 256 different current levels from typically 0mA to 30mA. When in the BLED strobe mode, it is suggested that setting OCP to 1.8A by register 0xA1[2:1] to avoid easier trigger OCP. The strobe currents are adjusted via the register for flash brightness. Strobe mode LED current is activated by setting register 0xAA [7:0]. When the backlight strobe function timeout is enable, it can set 7 bit programmable from 16ms to 2048ms in 16ms/code.

When backlight strobe mode is set, PWM control will be disabled and backlight current set to Bled_Strobe_Current. After strobe function timeout, bled_flash_mode set to 00 and return to backlight normal operation. The strobe current, strobe ramp up and ramp down can be set by the following table.

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3.43 Over-Voltage Protection (Open-circuit LED, or Any Open-Circuit)

The MT6371 provides an internal open-circuit LED, or any open-circuit protection to limit its output voltage. The OVP function prevents the MT6371 from being damaged when an open-circuit or open circuit condition occurs. Once the open circuit condition is removed, and the MT6371 will return to normal operation.

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3.44 LDO

A built-in low dropout linear regulator (LDO) provides a programmable output voltage and supplies output current of 600 mA, which enables a cost-effective solution to drive a vibration motor with ceramic output capacitors. The LDO output voltage can be programmed from 1.6V to 4V in a step of 200mV.

The LDO can be used to drive an external DC motor also referred to as Eccentric Rotating Mass (ERM) motor, in mobile device applications. The driver has fast response time if LDO_EN becomes active. A vibration kick can be produced by reversing the motor spin direction to produce a sharp transient and stop the motor quickly. When programming the LDO to a lower output voltage, the motor is further protected from being overdriven.

A small 2.2μF bypass ceramic capacitor is required to be connected directly between LDO_VIN pin and GND pin, and another 2.2μF ceramic bypass capacitor should be place in close proximity across the LDO_VOUT pin and the GND pin. The LDO output voltage setting is stored in the registers depending on the mode selected, haptic or vibrate respectively. The LDO also includes an internal circuit for short-circuit and over-current protection.

If the LDO is unused, LDO_VIN should connect to VSYS, and the REG0x81[7] should set 0.

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3.45 I²C Interface

The following table shows the MT6371 unique address as a PMU or PD slave to AP, respectively.

PMU Slave Address			
MSB	LSB	R/W Bit	R/W
011010	0	1/0	69/68
PD Slave Address			
MSB	LSB	R/W Bit	R/W
100111	0	1/0	9D/9C

The I²C interface bus must be connected to a resistor 2.2kΩ to power node and independent connection to processor, individually. The I²C interface also supports High-Speed (HS) mode for data transfer rate up to 3.4Mbits. The I²C timing diagrams are listed below.

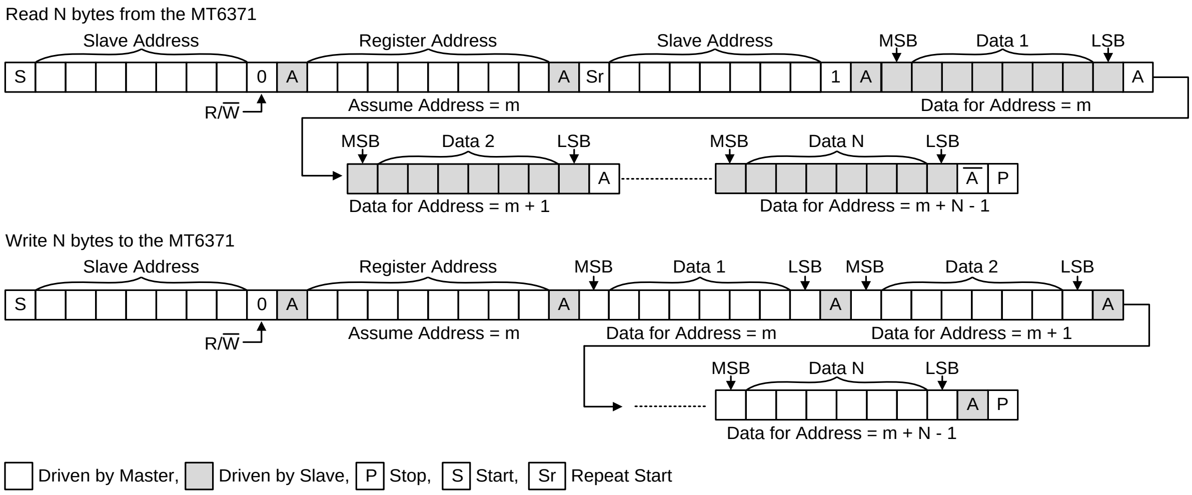

Figure 3-29. I²C timing diagrams

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3.46 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-91B 4.22x4.14 (BSC) package, the thermal resistance, θ_{JA}, is 22.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (22.4°C /W) = 4.46W for a WL-CSP-91B 4.22x4.14 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3-30 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

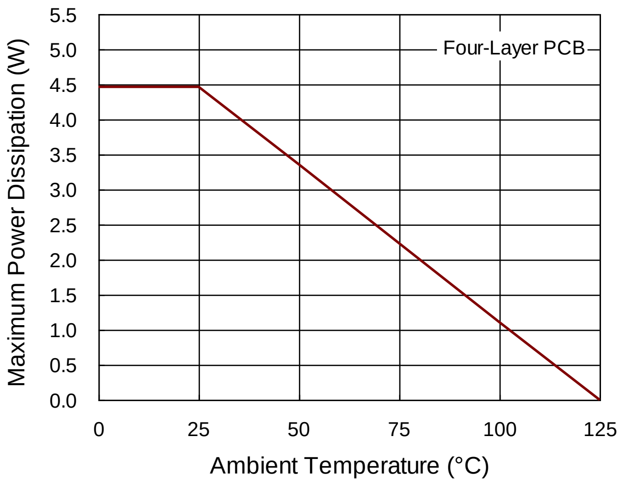

Figure 3-30. Derating curve of maximum power dissipation

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3.47 Layout Considerations

The PCB layout is an important step to maintain the high performance of the MT6371. Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the MT6371 through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the MT6371, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide, short and two layers as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Connect the AGND and PGND to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the output capacitors to the feedback network of each channel to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

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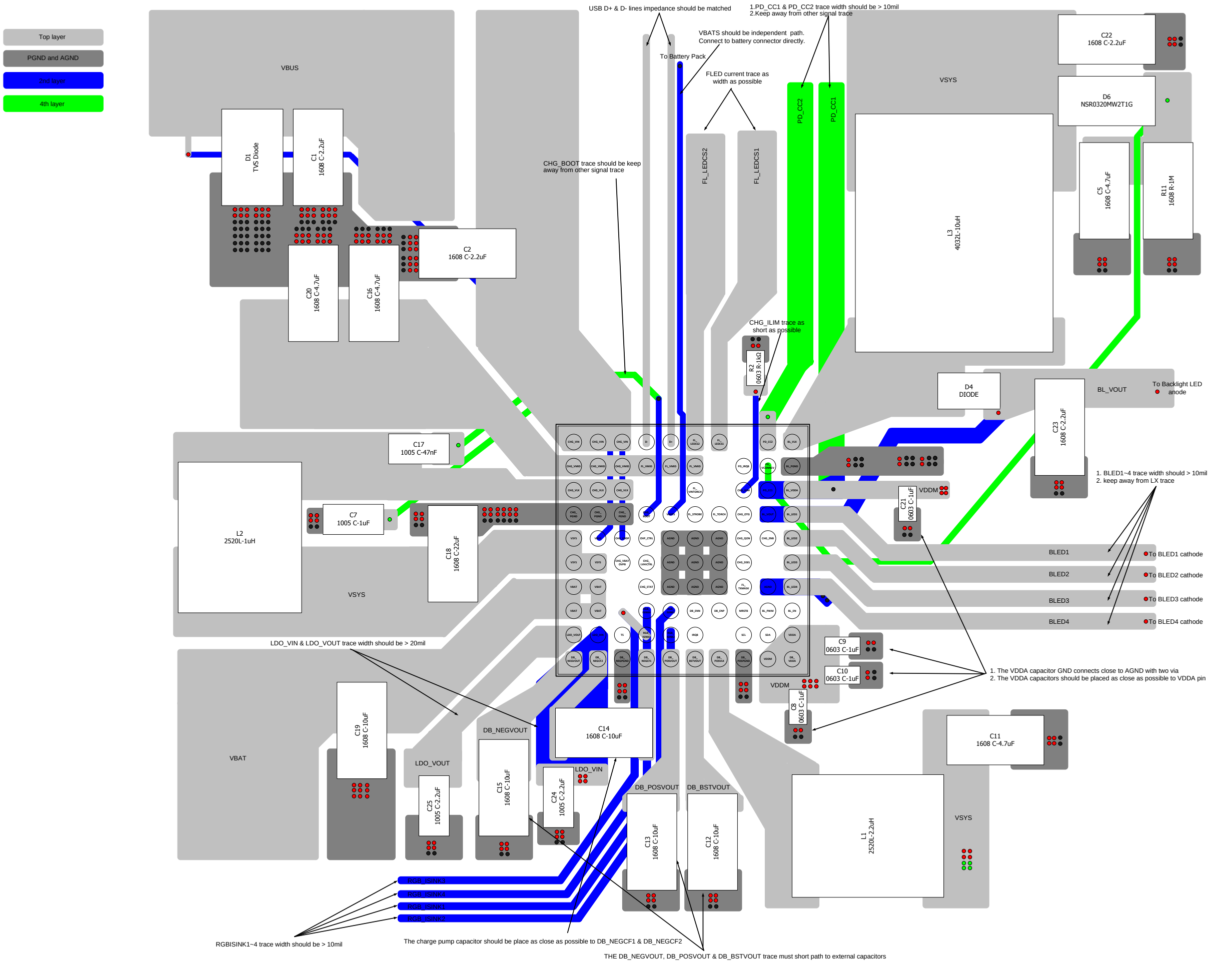
3.48 Top Layer

1. FL_VMID needs to connect to CHG_VMID and places C20 on the top layer.
2. Charger output needs to connect to Battery power path and the Battery power path should be wide, short and thick to prevent IR drop.
3. There should be an independent path from BATS pin to battery+ connector. It is to achieve Kelvin-sense input for battery voltage measurement. Besides, the path should be as short as possible.
4. Tie to the AGND and PGND to a strong ground plane on the top layer.



(a) Without external OVP function

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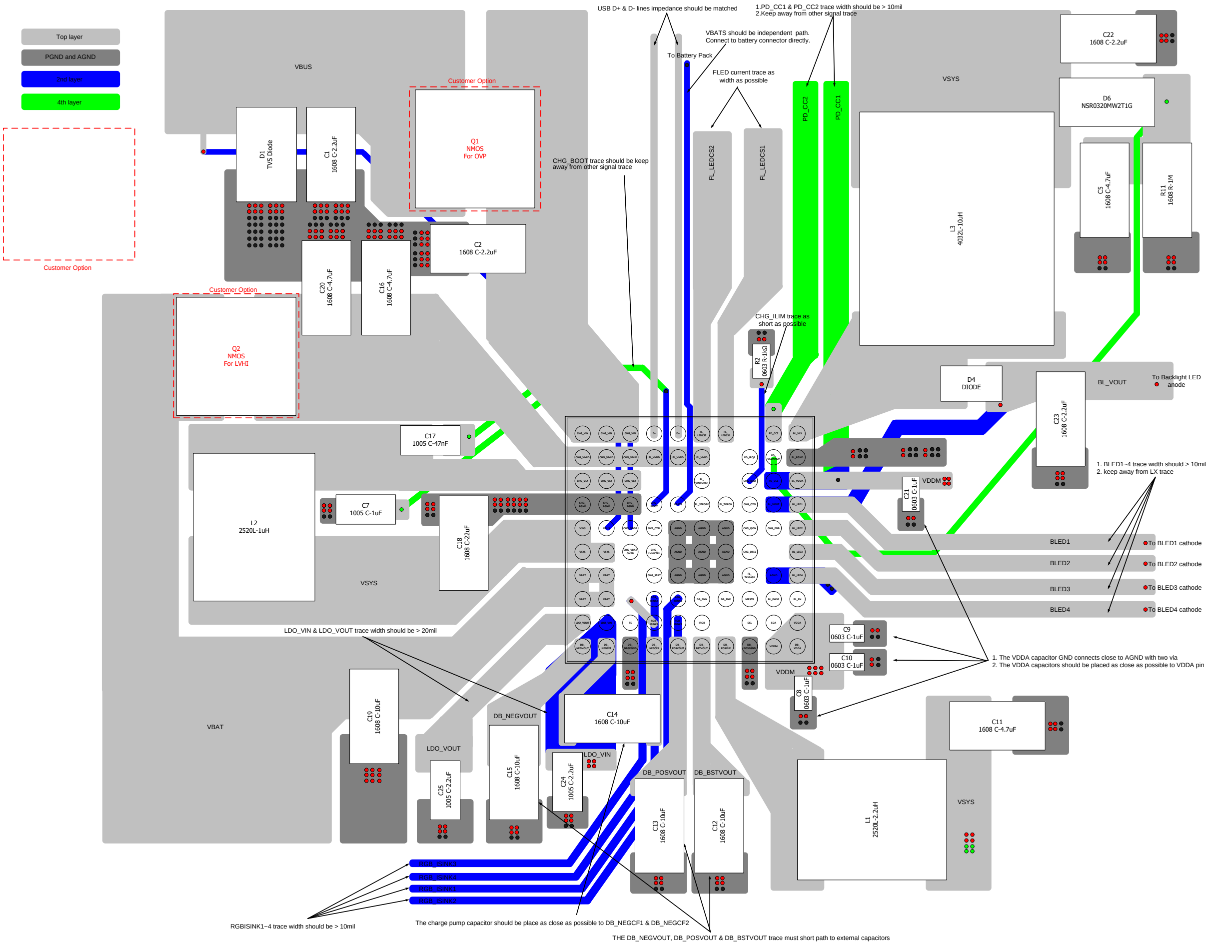

(b) With external OVP function

Figure 3-31. PCB layout guide

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4 Functional Descriptions

4.1 General Descriptions

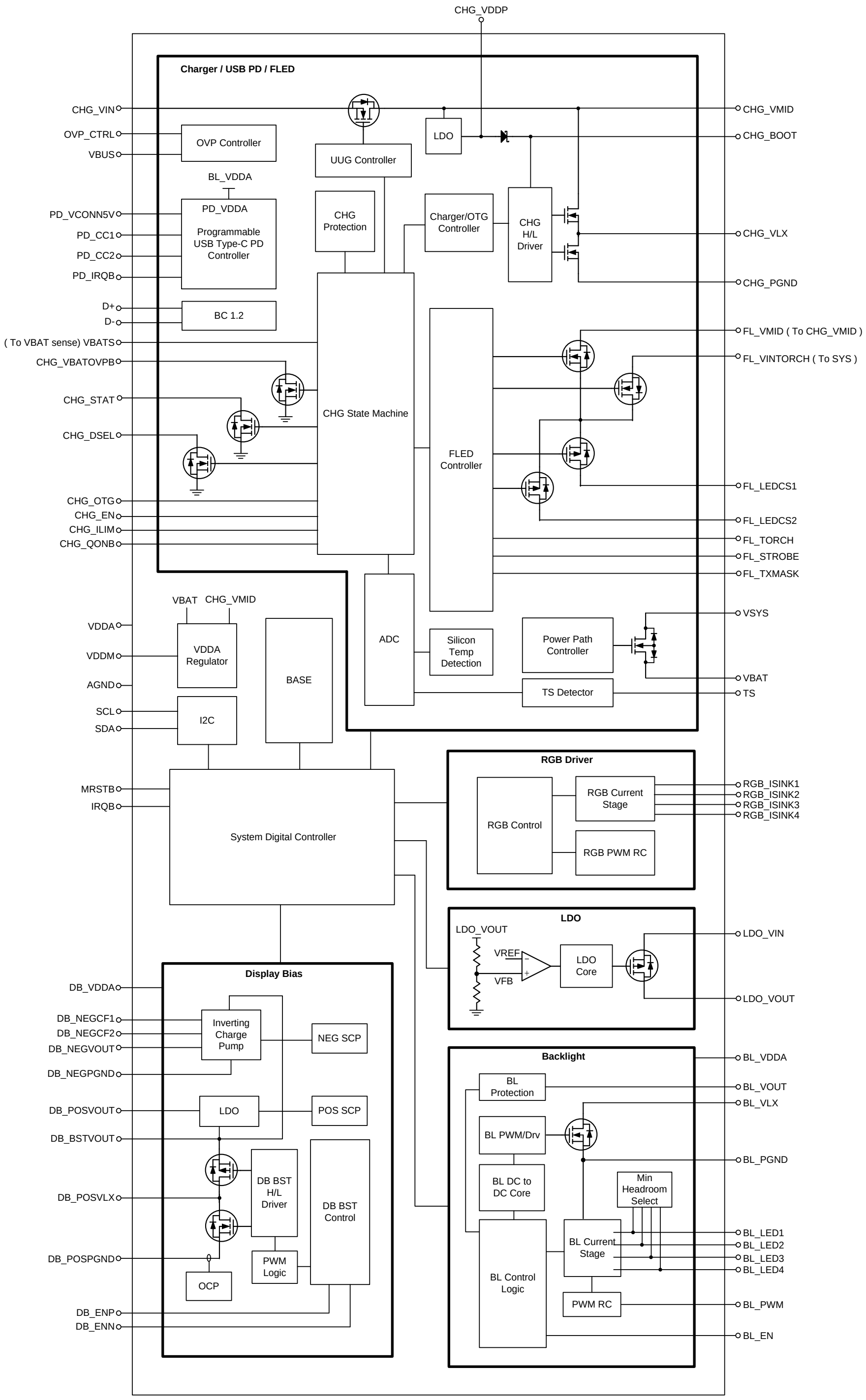

Figure 4-1. MT6371 functional block diagram

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Table 4-1. Control pin description

Part	Pin Name	Pin Description	Pin Type	I^2C Controlled	Pin Connection Suggestion When Unused
Top	MRSTB	Manual reset input for hardware reset.	Input/Active-Low (Default: Disable)	Yes	Floating
	SDA	I^2C interface serial data input/output. Open-drain. An external pull-up resistor is required.	Input/Output /Open-Drain	Yes	
	SCL	I^2C interface serial clock input. Open-drain. An external pull-up resistor is required.	Input/Output /Open-Drain	Yes	
	IRQB	Interrupt output, active-low open-drain, to request the processor to read the registers.	Output/Open-Drain	No	
	PD_IRQB	Interrupt output, active-low open-drain, to request the processor to read the registers.	Output/Open-Drain	No	Floating
Charger	CHG_ENB	Charger enable input, active-low.	Input/Active-Low	Yes	Tie to ground to enable charger
	CHG_OTG	OTG boost mode enable control, active-high. Act with OTG_PIN_EN.	Input/Active-High	Yes	Floating
	CHG_STAT	Charge status indication, open-drain output that indicates charge is in progress when held low and charge is finished when held High. If any fault occurs, CHG_STAT will blink at the frequency of 1Hz. Connect a 2.2k to 10kΩ pull-up resistor.	Output/Open-Drain	No	Floating
	CHG_DSEL	Open-drain output. When the device starts to detect input supply source, CHG_DSEL drives Low to indicate that detection is in progress and the device needs to take control of the D+ and D- signals. When detection is completed, CHG_DSEL holds Low if DCP (Dedicated Charging Port) or HVDCP adapter is detected. CHG_DSEL returns to High if SDP (Standard Downstream Port) or CDP (Charging Downstream Port) is detected.	Output/Open-Drain	No	Floating
Charger	CHG_VBATOVPB	Battery over-voltage protection (BAT OVP) indication, open–drain and active-low output: Low if BAT OVP occurs, and High, otherwise.	Output/Open-Drain	No	Floating
	CHG_QONB	Internal BATFET enable control input. In shipping mode, CHG_QONB is pulled Low for the duration of $t_{QONB_EXIT_SHIP_CHG}$ (typical 0.9s) to exit shipping mode.	Input/Active-Low	No	Floating
Flash	FL_TORCH	Flash LED Torch mode enable Input.	Input/Active-High	Yes	Short to ground
	FL_STROBE	Flash LED Strobe mode enable input.	Input/Active-	Yes	Short to

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Part	Pin Name	Pin Description	Pin Type	I²C Controlled	Pin Connection Suggestion When Unused
			High		ground
	FL_TXMASK	Configurable power amplifier synchronization input or configurable active-high torch mode enable. Connect an internal pull-down resistor of 400kΩ between FL_TXMASK and ground.	Input/Active-High (Default)	No	Short to ground
Backlight	BL_EN	Backlight enable control input.	Input/Active-High	Yes	Short to ground
	BL_PWM	Backlight PWM dimming control input.	Input	No	Short to ground
Display Bias	DB_ENP	Enable control input for DB_POSVOUT.	Input/Active-High	Yes	Short to ground
	DB_ENN	Enable control input for DB_NEGVOUT.	Input/Active-High	Yes	Short to ground

Table 4-2. If a channel is unused, follow the setting instructions as below.

Unused Part	Unused Function	Unused Pin Name	Pin Connection (Short to ground/Floating/Others)
OVP	All functions	VBUS	Short to CHG_VIN
		OVP_CTRL	Floating
Charger	Battery temperature sensing	TS	Connect a 50kΩ resistor to CHG_VDDP and a 50kΩ resistor to ground
	Input current limit setting	CHG_ILIM	Short to ground
	D+/D- Detection	D+	Floating
		D-	Floating
PD	All functions	CC1	Floating
		CC2	Floating
		PD_VCONN5V	Short to ground
Flash	All functions	FL_VINTORCH	Short to VSYS
		FL_VMID	Short to VMID
		FL_LEDCS1	Floating
		FL_LEDCS2	Floating
		FL_TORCH	Short to ground
		FL_STROBE	Short to ground
		FL_TXMASK	Short to ground
	Channel 1 only	FL_LEDCS1	Floating
	Channel 2 only	FL_LEDCS2	Floating
Display Bias	All functions	DB_VDDA	Short to VDDM
		DB_POSVLX	Floating
		DB_POSPGND	Short to ground
		DB_BSTVOUT	Floating
		DB_POSVOUT	Floating
		DB_NEGCF1	Floating
		DB_NEGCF2	Floating

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Unused Part	Unused Function	Unused Pin Name	Pin Connection (Short to ground/Floating/Others)
		DB_NEGVOUT	Floating
		DB_NEGPGND	Short to ground
		DB_ENP	Short to ground
		DB_ENN	Short to ground
Backlight	All functions	BL_VDDA	Short to VDDM
		BL_VLX	Floating
		BL_VOUT	Floating
		BL_PGND	Short to ground
		BL_LED1	Floating
		BL_LED2	Floating
		BL_LED3	Floating
		BL_LED4	Floating
		BL_PWM	Short to ground
		BL_EN	Short to ground
	Channel 1 only	BL_LED1	Floating
	Channel 2 only	BL_LED2	Floating
	Channel 3 only	BL_LED3	Floating
	Channel 4 only	BL_LED4	Floating
LDO	All functions	LDO_VIN	Short to VSYS
		LDO_VOUT	Floating
RGB	Channel 1 only	RGB_ISINK1	Floating
	Channel 2 only	RGB_ISINK2	Floating
	Channel 3 only	RGB_ISINK3	Floating
	Channel 4 only	RGB_ISINK4	Floating

Table 4-3. BOM list

Reference	Q'ty	Part Number	Description	Package	Manufacturer
D1	1	PTVSHC3N12VU	TVS Diode (For surge 100V/200V/300V/450V)	DFN 2x2	Prisemi
		ESD5641D12	TVS Diode (For surge 100V/200V/300V)	DFN 2x2	Willsemi
		ESD56241D12	TVS Diode (For surge 100V/200V/300V/450V)	DFN 2x2	Willsemi
Q1	1	DMN3016LFDF	N-Channel 30V VGS±20V MOSFET	DFN 2x2	DIODES
		DMT3020LFDF	N-Channel 30V VGS±20V MOSFET	DFN 2x2	DIODES
D2, D3	2	ELCH08-NB5565J6J8283910-F1S	Flash LED	2x1.6	Everlight
D4	1	NSR05F40NXT5G	SCHOTTKY DIODE	0402	On-semi
		SDM1A40CSP	SCHOTTKY DIODE	0402	DIODES
D5	1	AZ5315-02F	TVS Diode	DFN1006P3X	Amazing Micro
D6	1	PTVSHC3D4V5B	TVS DIODE(For surge 250V)	SOD–323	Prisemi
		PTVSHC3D4V5BH	TVS DIODE(For surge 250V)	SOD–323	Prisemi

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Reference	Q'ty	Part Number	Description	Package	Manufacturer
		ESD56151W04	TVS DIODE(For surge 250V)	SOD–323	Willsemi
C1, C2	2	GRM188R6YA225KA12	2.2μF/0603/35V/X5R	0603	MURATA
C23	1	GRM188R61H225KE11	2.2μF/0603/50V/X5R	0603	MURATA
C3, C4	2	GRM0335C1E331GA01	330pF/0201/25V/C0G	0201	MURATA
C5, C11	2	GRM185R61A475KE11	4.7μF/0603/10V/X5R	0603	MURATA
C6	1	GRM033R60J104KE19D	100nF/0201/6.3V/X5R	0201	MURATA
C7, C8, C9, C10, C21	5	GRM033R61A105ME1	1μF/0201/10V/X5R	0201	MURATA
C12, C13, C14, C15, C19	5	GRM188R61A106KAAL	10μF/0603/10V/X5R	0603	MURATA
C16, C20	2	GRM188R61E475KE11	4.7μF/0603/25V/X5R	0603	MURATA
C17	1	GRM155B31E473KA87	47nF/0402/25V	0402	MURATA
C18, C22	2	GRM187R61A226ME15	22μF/0603/10V/X5R	0603	MURATA
C24	1	GRM155R61A225KE95	2.2μF/0402/10V/X5R	0402	MURATA
C25	1	GRM153R60J225ME95	2.2μF/0402/6.3V/X5R	0402	MURATA
L1	1	DFE252012R-H-2R2M	2.2μH/2520/DCR = 75mΩ	2520	TOKO
L2	1	DFE252012F-H-1R0M	1μH/2520/DCR = 33mΩ	2520	TOKO
		CIGT252010EH1R0MNE	1μH/2520/DCR = 30mΩ	2520	Samsung
L3	1	MDMK4040T100MM	10μH/4040/DCR = 280mΩ	4040	Taiyo
R	6	RM02FTN2201	2.2K/0201/1%	0201	TA-I
R2	1	RR0306S-6980-FNH	698/0201/1%	0201	Cyntec
R11	1	RM02FTN1004	1M/0201/1%	0201	TA-I

Table 4-4. Protection list

Part	Protection Type	Threshold (Typical Value)	Deglitch Time	Protection Method	Reset Method
TOP	VDDA UVP	$V_{DDA} < V_{VDDA_UVLO}$	32μs	VDDA UVLO shutdown selection by (0x0E, bit[7:4])	$V_{DDA} > V_{VDDA_UVLO} + V_{VDDA_UVLO_HYS}$ Latch-off
	VDDA OVP	$V_{DDA} > V_{VDDA_OVP}$	32μs	VDDA OVP shutdown selection by (0x0E, bit[3:0])	V_{DDA} < 5.3V Latch-off
	OTP	Temperature > 160°C	0	OTP shutdown selection by (0x0F, bit[7:4])	Temperature < 140°C, Latch-off
Charger	Sleep Mode	V_{BUS} falling, V_{BUS}-V_{BAT} < 40mV	0	Charger shutdown	VBUS rising , VBUS - VBAT > 100mV
	VIN Bad Adapter	V_{BUS} < 3.8V	32ms	Sink 50mA current per 2s and keep to check whether the adapter is good or not	VBUS > 3.95V
	VIN UVLO	V_{BUS} < 3.15V	5μs	Charger shutdown	VBUS > 3.3V
	CHG_VIN OVP	V_{CHG_VIN} > 14.5V	0	Charger shutdown	CHG_VIN < 14.25V
	VBAT OVP	(V_{BAT}-V_{OREG_CHG})/V_{OREG_CHG} >	0	Stop charging	(V_{BAT}-V_{OREG_CHG})/V_{ORE}

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Part	Protection Type	Threshold (Typical Value)	Deglitch Time	Protection Method	Reset Method
		108%			G_CHG < 2%
	Thermal Regulation Threshold	Temperature > 120°C	0	Charging current is limited by thermal loop	N/A
	System OVP	V_{SYS} > 5.25V	0	Buck stop switching	VSYS < 4.95
	System UVP	V_{SYS} < 2.4V	2ms	Charger shutdown (Optional, 0x1B [5])	VSYS > 2.55
	Buck OCP Current	I_{CHG_VLX} > 6A I_{CHG_VLX} > 8A	0	OCP = 6A/8A selection by (0x1D, bit[2])	I_{CHG_VLX} < 6A I_{CHG_VLX} < 8A
	OTG OLP	I_{OUT} > 0.5 to 3A (selected by (0x1A, bit[2:0]))	4ms	Start to hiccup	IOUT < 0.5 to 3A
	OTG VMIDOVP	V_{CHG_VMID} > $V_{MIDOVP_OTG_CHG}$	0	Boost stop switching	V_{CHG_VMID} < $V_{MIDOVP_OTG_CHG}$ - $V_{MIDOVP_OTG_HYS_CHG}$
	OTG VBATUVP	V_{BAT} < 2.8V	512µs	Leave OTG mode	V_{BAT} < 3.2V
	OTG OCP	I_{CHG_VLX} > 3A, 4A, 5A or 6A	0	Higher_OCP_BST = 3A, 4A, 5A or 6A selection by (0x1F, bit[2:1])	I_{CHG_VLX} < 3A, 4A, 5A or 6A
	Jeita HOT Threshold	the ratio of VLDO < 34.5%	0	Stop charging	the ratio of VLDO > 36%
	Jeita WARM Threshold	the ratio of VLDO < 45%	0	ICHG/2, VOREG-0.2V	the ratio of VLDO > 46.5%
	Jeita COOL Threshold	the ratio of VLDO > 68.5%	0	ICHG/2, VOREG-0.2V	the ratio of VLDO < 67%
	Jeita COLD Threshold	the ratio of VLDO > 73.5%	0	Stop charging	the ratio of VLDO < 72%
PD	VCONN OCP	VCONN > 600mA	60µs	VCONN OCP shutdown selection by (0x93, bit[7:6])	Clear INT (1.0x1F, bit[1] 2.0x11, bit[1])
	VCONN OVP	VCONN > 6V	60µs	VCONN shutdown	Clear INT (1.0x1F, bit[7] 2.0x11, bit[1])
OVP_ CTRL	OVP	V_{BUS} > 16.5V	0.2µs	Turn off EXMOS	V_{BUS} < 16.3V
	UVP	V_{BUS} < 2.6V	2µs	Turn off EXMOS	V_{BUS} > 2.7V
FL	LEDCS Short	V_{FL_LEDCSx} < 1V (typ.)	2.5ms	FLED shutdown	V_{FL_LEDCSx} > 1V (typ.)
	Strobe Mode FL-CHG_VIN OVP	VCHG_VIN ≥ 5.6V (typ.)	5µs	FLED shutdown	VCHG_VIN ≤ 5.3V (typ.)
DB	POS Short Flag	VDB_POSVOUT < 0.8 x DB_VPOS	32num during 500µs	a. 0xB1[7] = 0 (default) Report only. Ipos limited by Iocp,pos. b. xB1[7] = 1 (HICCUP Mode) Ipos limited by Iocp,pos. If short event is over 2ms, POS will be turned off.	a. 0xB1[7] = 0 (default) Short event released Flag is R/C b. 0xB1[7] = 1 (HICCUP Mode) POS is auto-recovery and re-soft-start after POS is turned off

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Part	Protection Type	Threshold (Typical Value)	Deglitch Time	Protection Method	Reset Method
					40ms.
	NEG short Flag	VDB_NEGVOUT > 0.25 - 0.8 x DB_VNEG	32num during 500µs	a. 0xB1[7] = 0 (default) Report only. Ineg limited by Iocp,neg. b. 0xB1[7] = 1 (HICCUP Mode) Ineg limited by Iocp,neg. If short event is over 2ms, NEG will be turned off.	a. 0xB1[7] = 0 (default) Short event released Flag is R/C b. 0xB1[7] = 1 (HICCUP Mode) NEG is auto-recovery and re-soft-start after POS is turned off 40ms.
	POS OCP Flag	Ipos > Iocp,pos	32num during 500µs	Report only. Ipos limited by Iocp,pos	POS OCP event released. Flag is R/C.
	NEG OCP Flag	Ineg > Iocp,neg	32num during 500µs	Report only. Ineg limited by Iocp,neg.	NEG OCP event released. Flag is R/C.
	BST OCP Flag	Ibst > Iocp	32num during 500µs	Report only. Ibst limited by Iocp,bst.	BST OCP event released. Flag is R/C.
	BST OCP	IL > 1.1A (typ.)	0	Cycle by cycle detection. If OCP occurs, LG off.	IL < 1.1A
	OTP	Temperature > 160°C	0	Boost stop switching	Temperature < 140°C Hiccup
RGB	RGB Open-Circuit Flag	RGB_ISINKx Voltage < 100mV	28µs	Report only, Open_EN = 1 ISINK Voltage< open LED protection threshold	Open event Released Report flag RC
	RGB Short-Circuit Flag	RGB_ISINKx Voltage > VSYS-0.5V	28µs	Report only, Short_EN = 1 ISINK Voltage> short LED protection threshold	Short event Released Report flag RC
BL	BL_OVP	BL_OVP > 29V	32num during 500µs	selection by (0xA1, bit[7]) 0: OVP Shutdown 1: Report only, Backlight Boost Output > OVP Threshold	1. Shutdown: OVP event released and I²C enable again 2. Report only: OVP event released
	BL_OCP	BLED OC Current Limit > 1500mA	32num during 500µs	selection by (0xA1, bit[3]) 0: OC Limit Shutdown 1: Report only, Backlight Boost switch current > Current Limit Threshold	1. Shutdown: OCP event released and I²C enable again 2. Report only: OCP event released
	OTP	Temperature > 160°C	0	Boost stop switching and OTP shutdown selection by (0x0F, bit[7:4])	1. Shutdown: OTP event released and I²C enable again 2. Report only: OTP event

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Part	Protection Type	Threshold (Typical Value)	Deglitch Time	Protection Method	Reset Method
					released
LDO	Current Limit	PMOS current > 0.6A	0	V_{LDO_VOUT} goes low	Hiccup

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4.2 Register Table and Descriptions

PMIC Part Register Detailed Description

Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x00	DEV_INFO/ (Device Information)	7:4	VENDOR_ID	1111	R	Vendor Identification: Mediatek: 0101b
		3:0	CHIP_REV	0011	R	Chip Revision: 0001: 1st Version 0010: 2nd Version ... 1111: 15th Version
0x01	Core Ctrl 1	7	I2CSTMR_RST_EN	0	RW	I^2C Safe Timer enable for SDA/SCL low active. 0: Disable safe timer. 1: Enable safe timer.
		6:5	I2CSTMR_RST_TMR	00	RW	I^2C Safe Timer deglitch time. 00: 0.5Sec 01: 0.75Sec 10: 1Sec 11: 2Sec
		4	MREN	0	RW	GPIO: MRSTB reset function enable control 0: Disable 1: Enable (MRSTB pull low will start MRSTB Timer counting)
		3:1	MRSTB_TMR	011	RW	MRSTB debounce time selection 000: 0.75ms 001: 1ms 010: 1.25ms 011: 1.5ms 100: 1.75ms 101: 2ms 110: 2.25ms 111: 2.5ms
		0	MRSTB_RST_SEL	0	RW	I^2CSTMR_RST and MRSTB reset selection 0: Reset Hardware 1: Reset Register only
0x02	Core Ctrl 2	7	ALL_RST	0	RW	All registers and logic reset bit. 0: Don't reset all registers and logic. 1: Reset all registers and logic.
		6	CHG_RST	0		CHG registers and logic reset bit. 0: Don't reset CHG relative registers and logic. 1: Reset CHG relative registers and logic.
		5	FLED_RST	0		FLED registers and logic reset bit. 0: Don't reset FLED relative registers and logic. 1: Reset FLED relative

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						registers and logic.
		4	LDO_RST	0		LDO registers and logic reset bit. 0: Don't reset LDO relative registers and logic. 1: Reset LDO relative registers and logic.
		3	RGB_RST	0	RW	RGB registers and logic reset bit. RGB_PAS_CODE) 0: Don't reset RGB relative registers and logic. 1: Reset RGB relative registers and logic.
		2	BL_RST	0	RW	Backlight registers and logic reset bit. 0: Don't reset Backlight relative registers and logic. 1: Reset Backlight relative registers and logic.
		1	DB_RST	0	RW	DB registers and logic reset bit. 0: Don't reset DB relative registers and logic. 1: Reset DB relative registers and logic.
		0	REG_RST	0	RW	REG_PMU registers reset bits (Except to PD and start up by REG0x03 & REG0x04: RST_PAS_CODE) 0: Don't reset REG_PMU registers. 1: Reset REG_PMU registers. (Notice: This bit will be reset to "0" after reset procedure finish)
0x03	RST_PAS_CODE1	7:0	RST_PAS_CODE1	00000000	RW	RST_PAS_CODE1[7:0] /Passcode 1 for RST (except to PD): Set REG0x03 = 8'hA9 then set REG0x04 = 8'h96 , can start up REG0x02: ***_RST. To erase RST_PAS_CODE,REG0x02 won't work.
0x04	RST_PAS_CODE2	7:0	RST_PAS_CODE2	00000000	RW	RST_PAS_CODE2[7:0] /Passcode 2 for RST (except to PD): Set REG0x03 = 8'hA9 then set REG0x04 = 8'h96 , can start up REG0x02: ***_RST. To erase RST_PAS_CODE,REG0x02 won't work.

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x0B	IRQ_IND (IRQ Source Indicator)	7	CHG_EVT	0	R	Charger IRQ event indicator. 0: No IRQ event. : IRQ event occur.
		6	FLED_EVT	0	R	Flash LED IRQ event indicator. 0: No IRQ event. 1: IRQ event occur.
		5	LDO_EVT	0	R	LDO IRQ event indicator. 0: No IRQ event. 1: IRQ event occur.
		4	RGB_EVT	0	R	RGB IRQ event indicator. 0: No IRQ event. 1: IRQ event occur.
		3	BL_EVT	0	R	Backlight IRQ event indicator. 0: No IRQ event. 1: IRQ event occur.
		2	DB_EVT	0	R	DB IRQ event indicator. 0: No IRQ event. 1: IRQ event occur.
		1	BASE_EVT	0	R	BASE IRQ event indicator. 0: No IRQ event. 1: IRQ event occur.
		0	Reserved	0	R	Keep default value
0x0C	IRQ_MASK (IRQ Source Indicator Mask)	7	CHG_MASK	0	RW	Charger IRQ Mask Function. 0: Bypass IRQ event. 1: Mask IRQ event.
		6	FLED_MASK	0	RW	Flash IRQ Mask Function. 0: Bypass IRQ event. 1: Mask IRQ event.
		5	LDO_MASK	0	RW	LDO IRQ Mask Function. 0: Bypass IRQ event. 1: Mask IRQ event.
		4	RGB_MASK	0	RW	RGB IRQ Mask Function. 0: Bypass IRQ event. 1: Mask IRQ event.
		3	BL_MASK	0	RW	Backlight IRQ Mask Function. 0: Bypass IRQ event. 1: Mask IRQ event.
		2	DB_MASK	0	RW	DB IRQ Mask Function. 0: Bypass IRQ event. 1: Mask IRQ event.
		1	BASE_MASK	0	RW	BASE IRQ Mask Function. 0: Bypass IRQ event. 1: Mask IRQ event.
		0	Reserved	0	RW	Keep default value
0x0D	IRQ_SET (IRQ Setting)	7:6	INT_WDT	00	RW	Interrupt Watchdog timer. 00 : Disabled 01: 250ms 10: 500ms 11: 1000ms
		5:4	INT_DEG	01	RW	Interrupt forbidden pulse width timing. 00: 1ms 01: 2ms 10: 5ms

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						11: 10ms
		3:0	Reserved	0000	RW	Keep default value
0x0E	SHDN_CTRL1	7:4	VDDAUV_SHDN_SEL	0000	RW	VDDA UVLO shutdown selection (will disable channels and set sEN_CHx = 0) 0000: Disable VDDA UVLO shutdown function. 0001: Enable shutdown function and shutdown LDO only 0010: Enable shutdown function and shutdown RGB only 0011: Enable shutdown function and shutdown RGB / LDO 0100: Enable shutdown function and shutdown DB only 0101: Enable shutdown function and shutdown DB / LDO 0110: Enable shutdown function and shutdown DB / RGB 0111: Enable shutdown function and shutdown DB / RGB / LDO 1000: Enable shutdown function and shutdown BL only 1001: Enable shutdown function and shutdown BL / LDO 1010: Enable shutdown function and shutdown BL / RGB 1011: Enable shutdown function and shutdown BL / RGB / LDO 1100: Enable shutdown function and shutdown BL / DB 1101: Enable shutdown function and shutdown BL / DB / LDO 1110: Enable shutdown function and shutdown BL / DB / RGB 1111: Enable shutdown function and shutdown BL / DB / RGB / LDO

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x0E	SHDN_CTRL1	3:0	VDDAOVP_SHDN_SEL	1111	RW	VDDA OVP shutdown selection (will disable channels and set sEN_CHx = 0) 0000: Disable VDDA OVP shutdown function. 0001: Enable shutdown function and shutdown LDO only 0010: Enable shutdown function and shutdown RGB only 0011: Enable shutdown function and shutdown RGB / LDO 0100: Enable shutdown function and shutdown DB only 0101: Enable shutdown function and shutdown DB / LDO 0110: Enable shutdown function and shutdown DB / RGB 0111: Enable shutdown function and shutdown DB / RGB / LDO 1000: Enable shutdown function and shutdown BL only 1001: Enable shutdown function and shutdown BL / LDO 1010: Enable shutdown function and shutdown BL / RGB 1011: Enable shutdown function and shutdown BL / RGB / LDO 1100: Enable shutdown function and shutdown BL / DB 1101: Enable shutdown function and shutdown BL / DB / LDO 1110: Enable shutdown function and shutdown BL / DB / RGB 1111: Enable shutdown function and shutdown BL / DB / RGB / LDO

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x0F	SHDN_CTRL2	7:4	OT_SHDN_SEL	1111	RW	OT shutdown selection (will disable channels and set sEN_CHx = 0) 0000: Disable OTP shutdown function. 0001: Enable shutdown function and shutdown LDO only 0010: Enable shutdown function and shutdown RGB only 0011: Enable shutdown function and shutdown RGB / LDO 0100: Enable shutdown function and shutdown DB only 0101: Enable shutdown function and shutdown DB/LDO 0110: Enable shutdown function and shutdown DB/RGB 0111: Enable shutdown function and shutdown DB/RGB/LDO 1000: Enable shutdown function and shutdown BL only 1001: Enable shutdown function and shutdown BL/LDO 1010: Enable shutdown function and shutdown BL/RGB 1011: Enable shutdown function and shutdown BL/RGB/LDO 1100: Enable shutdown function and shutdown BL/DB 1101: Enable shutdown function and shutdown BL/DB/LDO 1110: Enable shutdown function and shutdown BL/DB/RGB 1111: Enable shutdown function and shutdown BL/DB/RGB/LDO
		3:0	Reserved	0000	RW	Keep default value
0x10	OSC_CTRL	7:2	Reserved	000010	RW	Keep default value
		1	FON_ENBASE	0	RW	Force BASE to turn on or not 0: BASE turn on according to system application 1: Force BASE to turn on
		0	FON_OSC	0	RW	Force OSC to turn on or not 0: OSC turn on according to system application

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						1: Force OSC to turn on
0x11	CHG_CTRL1	7	SEL_SWFREQ	0	RW	The switching frequency selection bit (Charger/OTG) 0: The switching frequency is 1.5MHz. 1: The switching frequency is 0.75MHz.
		6	FIXFREQ	0	RW	Charger switching frequency 0: Charger switching frequency will be varied if V_{BUS} is close to V_{BAT} (default) 1: Charger switching frequency is fixed
		5	OSCSS_EN	0	RW	Charger spread spectrum enable 0: Disable 1: Enable
		4	STAT_EN	1	RW	Charger STAT pin function 0: Disable 1: Enable
		3	Force_Sleep	0	RW	Force Sleep to reduce I (VIN_CHG) 0: Normal 1: Force Sleep
		2	HZ	0	RW	Hz selection 0: No high impedance mode 1: High impedance mode
		1	OTG_PIN_EN	0	RW	Boost mode enable with OTG pin 0: Enable Boost mode by OPA_MODE 1: Enable Boost by both OPA_MODE bit and OTG pin
		0	OPA_MODE	0	RW	Boost mode enable 0: Charge mode 1: Boost mode for OTG
0x12	CHG_CTRL2	7	SHIP_MODE	0	RW	Shipping mode enable, force BATFET OFF 0: Allow BATFET turn on 1: Force BATFET turn off
		6	BATDET_DIS_DLY	0	RW	BATFET turn off delay 0: BATFET turn off immediately 1: BATFET turn off with 10s delay after SHIP_MODE bit is set
		5	Reserved	0	RW	Reserved
		4	TE	0	RW	Termination enable 0: Disable charge current termination 1: Enable charge current termination
		3:2	IINLMTSEL	00	RW	Input current limit selection bit 00: AICR = 3.25A

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						01: CHG_TYP results is applied 10: IAICR[5:0] results is applied 11: Input limit is set by the lower level of these three
		1	CFO_EN	1	RW	Charger and OTG enable 0: CFO is disabled 1: CFO is enabled
		0	CHG_EN	1	RW	Charging enable 0: CHG is disabled 1: CHG is enabled
0x13	CHG_CTRL3	7:2	IAICR	001000	RW	AICR setting 000000: 100mA 000001: 150mA 000010: 200mA 000011: 250mA ... 001000: 500mA 001001: 550mA ... 100110: 2A ... 11101 : 3A ... 111111: 3.25A
		1	AICR_EN	1	RW	AICR loop enable 0: AICR loop disable 1: AICR loop enable
		0	ILIM_EN	1	RW	ILIM function enable 0: ILIM function disable 1: ILIM function enable
0x14	CHG_CTRL4	7:1	VOREG	0011110	RW	Battery regulation voltage. The delta-V of the battery regulation voltage is 10mV. 0000000: 3.9V 0000001: 3.91V 0000010: 3.92V 0000011: 3.93V ... 0011101: 4.19V 0011110: 4.2V 0011111: 4.21V ... 0101100: 4.34V 0101101: 4.35V 0101110: 4.36V ... 1010001: 4.71V 1010001~1111111: 4.71V
		0	Reserved	0	RW	Keep default value
0x15	CHG_CTRL5	7:2	VOBST	011001	RW	OTG regulation voltage. The delta-V of the OTG regulation voltage is 25mV. 000000: 4.425V 000001: 4.45V 000010: 4.475V ... 010111: 5V

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						011000: 5.025V 011001: 5.05V 011010: 5.075V 011011: 5.1V ... 111000: 5.825V 111000~111111: 5.825V
		1:0	THREG	11	RW	Charger thermal regulation threshold 00: 60ºC 01: 80ºC 10: 100ºC 11: 120ºC
0x16	CHG_CTRL6	7:1	VMIVR	0000101	RW	Input MIVR threshold setting 0000000: 3.9V 0000001: 4V 0000010: 4.1V 0000011: 4.2V 0000100: 4.3V 0000101: 4.4V 0000110: 4.5V ... 0011110: 6.9V 0011111: 7V ... 0110010: 8.9V 0110011: 9V ... 1010000: 11.9V 1010001: 12V ... 1011111: 13.4V 1100000~1111111: 13.4V
		0	MIVR_EN	1	RW	MIVR loop enable 0: MIVR loop disable 1: MIVR loop enable
0x17	CHG_CTRL7	7:2	ICHG	010011	RW	Regulated charge current 000000: Reserved ... 000011: Reserved 000100: 0.5A ... 001000: 0.9A 001001: 1A 001010: 1.1A ... 010010: 1.9A 010011: 2A ... 011100: 2.9A 011101: 3A ... 100110: 3.9A 100111: 4A ... 110000: 4.9A 110001: 5A 110010~111111: 5A Note : When ICHG is set above 2.5A, recommend

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						the OCP to set higher level. (Addr 0x1D[2] = 1)
		1:0	EOC_TIMER	00	RW	EOC back-charging time 00: 0mins 01: 30mins 10: 45mins 11: 60mins
0x18	CHG_CTRL8	7:4	VPREC	1010	RW	Pre-charge voltage threshold (Rising) 0000: 2V 0001: 2.1V 0010: 2.2V 0011: 2.3V 0100: 2.4V 0101: 2.5V 0110: 2.6V 0111: 2.7V 1000: 2.8V 1001: 2.9V 1010: 3.0V 1011: 3.1V 1100: 3.2V 1101: 3.3V 1110: 3.4V 1111: 3.5V
		3:0	IPREC	0001	RW	Pre-charge current level 0000 : 100mA 0001: 150mA 0010: 200mA 0011: 250mA 0100: 300mA 0101: 350mA 0110: 400mA 0111: 450mA 1000: 500mA 1001: 550mA 1010: 600mA 1011: 650mA 1100: 700mA 1101: 750mA 1110: 800mA 1111: 850mA
0x19	CHG_CTRL9	7:4	IEOC	0011	RW	End-of-charge current (IEOC) setting 0000: 100mA 0001: 150mA 0010: 200mA 0011: 250mA 0100: 300mA 0101: 350mA 0110: 400mA 0111: 450mA 1000: 500mA 1001: 550mA 1010: 600mA 1011: 650mA 1100: 700mA 1101: 750mA 1110: 800mA 1111: 850mA

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		3	EOC_EN	1	RW	IEOC (charge current termination) enable/disable 0: Disable 1: Enable
		2:0	CHG_TDEG_EOC	100	RW	EOC deglitch time 000: 32μs 001: 64μs 010: 128μs 011: 256μs 100: 2ms 101: 4ms 110: 8ms 111: 16ms
0x1A	CHG_CTRL10	7:4	LBP	0101	RW	Low battery protection voltage selection (falling edge threshold, hysteresis voltage = 0.4V) 0000: 2.3V 0001: 2.4V 0010: 2.5V 0011: 2.6V 0100: 2.7V 0101: 2.8V 0110: 2.9V 0111:3.0V 1000: 3.1V 1001: 3.2V 1010: 3.3V 1011 3.4V 1100: 3.5V 1101: 3.6V 1110: 3.7V 1111: 3.8V
		3	LBP_EN	1	RW	Low battery protection enable/disable 0: Disable 1: Enable
		2:0	OTG_OC	000	RW	OTG overload threshold of UUG Current 000: 0.5A 001: 0.7A 010: 1.1A 011: 1.3A 100: 1.8A 101: 2.1A 110: 2.4A 111: Reserved
0x1B	CHG_CTRL11	7	ADP_DIS	0	RW	Charger adapter detection disable 0: Adapter detection is enable 1: Adapter detection is disabled
		6	BATD_EN	0	RW	Charger battery detection when charge done 0: Battery detection is disabled 1: Battery detection is enabled

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		5	SYSUV_HW_SEL	1	RW	System UV protection selection bit 0: Switching is not turned off when System UVP 1: Switching is turned off when System UVP
		4:2	SYSREG	011	RW	System minimum regulation voltage 000: 3.3V 001: 3.4V 010: 3.5V 011: 3.6V 100: 3.7V 101: 3.8V 110: 3.9V 111: 4.0V
		1:0	VRECH	00	RW	Charging re-charge voltage threshold with VOREG 00 : 100mV 01: 200mV 10: 300mV 11: 400mV
0x1C	CHG_CTRL12	7:5	WT_FC	000	RW	Fast charge Timer 000: 4hrs 001: 6hrs 010: 8hrs 011: 10hrs 100: 12hrs 101: 14hrs 110: 16hrs 111: 20hrs
		4:3	WT_PRC	00	RW	Pre-charge Timer 00: 30mins 01: 45mins 10: 60mins 11: 60mins
		2	TMR2X_EN	0	RW	Double charger timer during MIVR, AICR, and thermal regulation 0: Disable 2x extended charger timer 1: Enable 2x extended charger timer
		1	TMR_EN	1	RW	Charger timer enable/disable 0: Disable 1: Enable
		0	TMR_PAUSE	0	RW	Timer control bit 0: Timer is active 1: Timer is pause
0x1D	CHG_CTRL13	7	CHG_WDT_EN	0	RW	Charger Watch dog timer enable/disable 0: Disable 1: Enable
		6	CHG_WDT_TRST	1	RW	Waiting timer to set REG0x12[1]: CFO_EN = 0, REG0x12[0]: CHG_EN = 0, REG0x11[1:0] = 00: OTG Disable and REG0x01[7]:

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						I²CSTMR_RST_EN = 1 after watchdog is asserted 0: 200ms 1: 500ms
		5:4	CHG_WDT	01	RW	Watch dog timer, from WDTEN is enabled to watchdog IRQ 00: 8s 01: 40s 10: 80s 11: 160s
		3	AJITA	0	RW	Charger ICHG current setting of JEITA 0: ICHG value is kept 1: ICHG value becomes half
		2	Higher_OCP	0	RW	Inductor peak current limit level of Buck mode 0: OCP = 6A 1: OCP = 8A
		1	UUG_ON	1	RW	UUG enable/disable control 0: Force UUG turn off 1: Allow UUG turn on
		0	slG_BSTmode	0	RW	Force VDDM power from VBAT 0: VDDM = max (internal LDO, VBAT) 1: VDDM = VBAT
0x1E	CHG CTRL 14	7	AICL_MEAS	0	RW	AICL measurement mechanism 0: No operation 1: Execute AICL measurement
		6:5	TDEG_ AICL_MEAS	00	RW	Comparator output deglitch time 00: 2ms 01: 4ms 10: 8ms 11: 16ms
		4:3	AICL_MAX_MEAS_INTVL	00	RW	Detection internal time 00: 50ms 01: 100ms 10: 200ms 11: 400ms
		2:0	AICL_VTH	101	RW	Detection comparator threshold 000: 4.1V 001: 4.2V 010: 4.3V 011: 4.4V 100: 4.5V 101: 4.6V 110: 4.7V 111: 4.8V
0x1F	CHG CTRL 15	7	ICHG_MEAS	0	RW	ICHG measurement mechanism 0: No operation 1: Execute ICHG measurement

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		6:3	ICHG_RPT	0000	R	Report the ICC measurement result
		2:1	Higher_OCP_BST	11	RW	Inductor peak current limit level of Boost Mode 00: OCP_BST = 3A 01: OCP_BST = 4A 10: OCP_BST = 5A 11: OCP_BST = 6A
		0	Reserved	0	RW	Reserved
0x20	CHG CTRL 16	7	cold_bat_chg_en	0	RW	0: COLD stop charging 1: COLD continue charging
		6	hot_bat_chg_en	0	RW	0: HOT stop charging 1: HOT continue charging
		5	Reserved	0	RW	Reserved
		4	JEITA_EN	1	RW	JEITA function enable/disable 0: Disable 1: Enable
		3	JEITA_COOL_ISET	0	RW	JEITA current setting in COOL region 0: Set Charge Current to ICHG /2 1: Set Charge Voltage to ICHG
		2	JEITA_WARM_ISET	0	RW	JEITA current setting in WARM region 0: Set Charge Current to ICHG /2 1: Set Charge Voltage to ICHG
		1	JEITA_COOL_VSET	0	RW	JEITA voltage setting in COOL region 0: Set Charge Voltage to CV-0.2V 1: Set Charge Voltage to CV
		0	JEITA_WARM_VSET	0	RW	JEITA voltage setting in WARM region 0: Set Charge Voltage to CV-0.2V 1: Set Charge Voltage to CV
0x21	CHG ADC	7:4	ADC_IN_SEL	0000	RW	ADC channel selection 0000: Reserved 0001: VBUS/5 0010: VBUS/2 0011: VSYS 0100: VBAT 0101: Reserved 0110: TS_BAT 0111: Reserved 1000: IBUS 1001: IBAT 1010: Reserved 1011: CHG_VDDP 1100: TEMP_JC 1101~1111: Reserved
		3:1	Reserved	000	RW	Reserved

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		0	ADC_START	0	RW	ADC start control 0: ADC conversion not active 1: Start ADC conversion (auto clear when conversion done)
0x22	Device Type	7	USBCHGEN	1	RW	USB charger detection flow enable/disable 0: Disable USB charger detection flow 1: Enable USB charger detection flow
		6	DCD Timeout EN	1	RW	0 : Disable DCD Timeout 1 : Enable DCD Timeout
		5:4	DCD_TIMEOUT	01	RW	Data contact detection timeout 00: 300ms 01: 600ms 10: 900ms 11: 1200ms
		3:0	Reserved	0000	RW	Reserved
0x24	DCP Control	7:2	Reserved	001000	RW	Reserved
		1	sEN_DCP	0	RW	Enable dedicate charging port 0: Disable 1: Enable
		0	Reserved	1	RW	Reserved
0x27	USB Status 1	7	Reserved	0	R	Keep default value
		6:4	USB Status	000	R	000: No VBUS 001: VBUS flow is under going 010: SDP (AICR = 500mA) 011: SDP NSTD (Unknown adapter, AICR = 500mA) 100: DCP (AICR = 3.25A) 101: CDP (AICR = 1.5A) 110: reserved 111: reserved
		3	CHGDET	0	R	0: Charger port is not detected 1: Charger port is detected
		2	DCDT	0	R	0: DCD Timeout event of BC detection not occurs 1: DCD Timeout event of BC detection occurs
		1:0	Reserved	00	R	Keep default value
0x2A	CHG_PUMP	7	PP_OFF_rst dis	0	RW	Disable / enable QON = 0 for 15s sys reset 0: Don't disable rst function (QON = 0 for 15s will reset system) 1: Disable rst function (QON = 0 will not reset system)
		6	sBCK_SWITCHING_EN	1	RW	Only charge buck enable/disable (allowing Boost operation) 0: Disable 1: Enable

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		5:2	Reversed	1000	RW	Reversed
		1	VG_LVL_SEL	0	RW	Charge pump pumping level selection 0: 5V 1: 10V
		0	VG_EN	0	RW	Charge pump enable/disable 0: Disable 1: Enable
0x2B	CHG CTRL 17	7	EN_PUMPX	0	RW	Enable MTK pump express pulse 0: Disable 1: Allow MTK pump express pulse
		6	PUMPX_2.0_1.0	0	RW	MTK pump express 2.0/1.0 enable 0: PE1.0 Enable 1: PE2.0 Enable
		5	PUMPX_UP_DN	0	RW	MTK pump express 1.0 voltage up/down enable 0: PE1.0 voltage down enable 1: PE1.0 voltage up enable
		4:0	PUMPX_DEC	00000	RW	MTK pump express 2.0 voltage request setting 00000: 5.5V 00001: 6V 00010: 6.5V ... 00111: 9V ... 01101: 12V ... 11101: 20V 11110: Adapter healthy self-testing 11111: Disable cable drop compensation
0x2C	CHG CTRL 18	7:6	Reserved	01	RW	Reserved
		5:3	BAT_COMP	000	RW	Battery IR compensation resistor setting 000: 0mΩ 001: 25mΩ 010: 50mΩ 011: 75mΩ 100: 100mΩ 101: 125mΩ 110: 150mΩ 111: 175mΩ
		2:0	VCLAMP	000		Battery IR compensation maximum voltage clamp 000: 0mV 001: 32mV 010: 64mV 011: 96mV 100: 128mV 101: 160mV 110: 192mV 111: 224mV
0x4A	CHG STAT	7:6	CHG_STAT	00	R	Charger status

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						00: ready 01: charge is in progress 10: charge is done 11: fault
		5	VBAT_LVL	0	R	Battery voltage level selection for 2 operation modes 0: in pre-charge mode 1: in fast-charge mode
		4	VBAT_TRICKLE	0	R	Battery voltage level for operation mode 0: Charger does not operate in trickle level 1: Charger operates in trickle level
		3	BOOST_STAT	0	R	Boost mode status 0: not in boost mode 1: boost mode
		2	BST_VBUSOVP_STAT	0	R	Boost mode VBUS OVP status 0: boost-mode VBUS OVP does not occur 1: boost-mode VBUS OVP occurs
		1	Reserved	0	R	Reserved
		0	ADC_STAT	0	R	ADC status 0: ADC is idle 1: ADC is under conversion
0x4B	CHG_NTC	7	Reserved	0	R	Reserved
		6:4	BAT_NTC_FAULT	000	R	BAT NTC fault status 000: Normal 010: Warm 011: Cool 101: Cold 110: Hot
		3:0	Reserved	000	R	Reserved
0x4C	ADC_DATA_H	7:0	ADC_CODEH	00000000	R	ADC code high byte
0x4D	ADC_DATA_L	7:0	ADC_CODEL	00000000	R	ADC code low byte
0x61	OVPCTRL	7:4	Reserved	0000	RW	Keep default value
		3	sFUN_OVPCTRL<3>	0	RW	0: VBUS de-bounce time is not bypassed (VBUSPOR time = 32ms) 1: VBUS de-bounce time is bypassed (VBUSPOR time = 8ms)
		2	sFUN_OVPCTRL<2>	0	RW	0: OVP level is 16.5V 1: OVP level is 5.8V
		1	sFUN_OVPCTRL<1>	0	RW	0: OVP function enable 1: OVP function disable except UV/OV flag
		0	Reserved	0	RW	Keep default value
0x62	VDDA Supply	7:2	Reserved	000000	RW	Reserved
		1:0	sVOVDDM_SEL<1:0>	01	RW	VDDM Output voltage setting: 11: 4.88V

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						10: 4.8V 01: 4.6V 00: 4.4V
0x70	FLED_CFG (FLED 1-2 Config)	7	TX_ActiveLevel	1	RW	TX Active Level selection : 0: Low Level 1: High Level
		6:5	TXSEL	00	RW	FLED TX function enable control bits 00: ALL FLEDs' TX function disable 01: FLED1's TX function enable and FLED2's disable 10: FLED1's TX function disable and FLED2's enable 11: ALL FLEDs' TX function enable
		4:2	Reserved	000	RW	Keep default value
		1	FLED_STRB_LES	0	RW	FLED strobe mode: level sensitive enable or rising edge trigger one-shot operation. 0: Level sensitive 1: Rising edge trigger
		0	Reserved	1	RW	Keep default value
0x72	FLED1_CTRL	7	Reserved	0	RW	Keep default value
		6:4	FLED1_TCL	000	RW	FLED1 timeout current level. 000: 25mA 001: 50mA ... 110: 175mA 111: 200mA If utra_istrb1 = 1 000 = 12.5mA 111 = 100mA
		3:0	Reserved	0000	RW	Keep default value
0x73	FLED_STRB_CTRL (FLED Strobe Control)	7	Reserved	0	RW	Keep default value
		6:0	FLED_STRB_TO	0100101	RW	FLED strobe timeout 0000000: 64ms 0000001: 96ms ... 0100101: 1248ms ... 1001001: 2400ms 1001010: 2432ms ... 1111111: 2432ms
0x74	FLED1_STRB_CTRL (FLED1 Strobe Control)	7	FLED1 ULTRA LOW ISTRB\ (utral_istrb1)	0	RW	0: Normal, 1: I(FLED1_ISTRB[6:0])/2 FLED1 Strobe current 0x74[6:0] 000,0000: 25mA 000,0001: 31.25mA ... 0111100: 400mA (default) ... 1110100: 750mA ... 1111111: 750mA

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		6:0	FLED1_ISTRB	0111100	RW	FLED1 strobe current 0000000: 50mA 0000001: 62.5mA ... 0111100: 800mA (default) ... 1110100: 1500mA ... 1111111: 1500mA
0x75	FLED1_TOR_CTRL (FLED1 Torch Control)	7:5	Reserved	000	RW	Keep default value
		4:0	FLED1_ITOR	00001	RW	FLED1 torch current 00000: 25mA 00001: 37.5mA ... 01111: 212.5mA ... 11110: 400mA
0x76	FLED2_CTRL	7	Reserved	0	RW	Keep default value
		[6:4]	FLED2_TCL	000	RW	FLED2 timeout current level. 000: 25mA 001: 50mA ... 110: 175mA 111: 200mA If utra_istrb2 = 1 000 = 12.5mA 111 = 100mA
		[3:0]	Reserved	0000	RW	Keep default value
0x78	FLED2_STRB_CTRL (FLED2 Strobe Control)	7	FLED2 ULTRA LOW ISTRB\ (utral_istrb2)	0	RW	0: Normal, 1: I(FLED2_ISTRB[6:0])/2 FLED2 Strobe current 0x74[6:0] 000,0000: 25mA 000,0001: 31.25mA ... 0111100: 400mA (default) ... 1110100: 750mA ... 1111111: 750mA
		6:0	FLED2_ISTRB	0111100	RW	FLED2 strobe current 0000000: 50mA 0000001: 62.5mA ... 0111100: 800mA (default) ... 1110100: 1500mA ... 1111111: 1500mA
0x79	FLED2_TOR_CTRL (FLED2 Torch Control)	7:5	Reserved	000	RW	Keep default value
		4:0	FLED2_ITOR	00001	RW	FLED2 torch current 00000: 25mA 00001: 37.5mA ... 01111 : 212.5mA ... 11110 : 400mA
0x7A	FLED_VMID TRK_CTRL1 (VMID Fix	7:6	Reserved	00	R	Reserved
		5:0	FLED_VMID	110111	RW	MID Regulation Level

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
	Mode Control)					(priority is higher than charger setting when EN_FLED = 1) 000000: 3.625V 000001: 3.65V 000010: 3.675V ... 110111: 5V ... 111110: 5.175V 111111: 5.2V
0x7B	FLED_VMID_RTM (VMID Voltage Read back)	7:6	Reserved	00	RW	Keep default value
		5:0	FLED_VMID_RTM	000000	R	Indicates actual MID Regulation voltage in tracking mode. 000000: 3.625V 000001: 3.65V 000010: 3.675V ... 110111: 5V ... 111110: 5.175V 111111: 5.2V
0x7C	FLED_VMID TRK_CTRL2 (Tracking Control)	7:3	Reserved	00000	RW	Keep default value
		2	FLED_TRK_CLK	0	RW	VMID tracking rage 0: 6kHz 1: 3kHz
		1:0	FLED_VTHREG	10	RW	Vreg setting: the dropout voltage between VMID and LEDCS1/2. 00: 250mV 01: 300mV 10: 350mV 11: 400mV
0x7E	FLED_EN (TORCH / STROBE)	7:4	Reserved	0000	RW	Keep default value
		3	FL_TORCH_reg	0	RW	FLED TORCH Mode enable control 0: disable FLED torch mode 1: enable FLED torch mode
		2	FL_STROBE_reg	0	RW	FLED STROBE Mode enable control 0: disable FLED strobe mode 1: enable FLED strobe mode Note: Reset to " 0 " after FLED_STROBE TimeOut
		1	FLCS1_EN	0	RW	FL_LEDCS1 Enable control 0: Disable FL_LEDCS1 1: Enable FL_LEDCS1
		0	FLCS2_EN	0	RW	FL_LEDCS2 Enable control 0: Disable FL_LEDCS2 1: Enable FL_LEDCS2
0x80	LDO_CFG (General LDO Configuration)	7	Reserved	0	RW	Keep default value
		6	LDO_OMS	1	RW	LDO output off mode state 0: Floating 1: Ground-discharged

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		5	LDO_VRC_EN	0	RW	LDO VRC Enable 0: Disable VRC function (Dynamic Voltage Ramp Control) 1: Enable VRC function
		4:3	LDO_VRC_LT	01	RW	LDO output pre/post-load time when output voltage setting change 00: Disable pre/post-loading time and pre/post-loading 01: 10µSec 10: 20µSec 11: 40µSec
		2:1	LDO_VRC	00	RW	LDO VRC Setting 00: 1Step/16µSec 01: 2Step/16µSec 10: 4Step/16µSec 11: 8Step/16µSec
		0	Reserved	0	RW	Keep default value
0x81	LDO_VOUT (General LDO Output)	7	LDO_EN	0	RW	LDO Enable 0: Disable 1: Enable
		6:4	Reserved	000	RW	Keep default value
		3:0	LDO_VOUT	1001	RW	LDO output voltage regulation, 200mV per Step. 0000: 1.6V 0001: 1.8V 0010: 2.0V ... 1000: 3.2V 1001: 3.4V ... 11XX: 4.0V
0x82	RGB1_DIM	7	Reserved	0	RW	Keep default value
		6:5	ISINK1_DIM_MODE	11	RW	ISINK1 Mode Select 00 = PWM Mode 01 = Breath Mode 1X = Register Mode
		4:0	ISINK1_DIM_DUTY	00000	RW	ISINK1 PWM Mode Dimming Duty = (N+1)/32 N = 0 to 31
0x83	RGB2_DIM	7	Reserved	0	RW	Keep default value
		6:5	ISINK2_DIM_MODE	11	RW	ISINK2 Mode Select 00 = PWM Mode 01 = Breath Mode 1X = Register Mode
		4:0	ISINK2_DIM_DUTY	00000	RW	ISINK2 PWM Mode Dimming Duty = (N+1)/32 N = 0 to 31
0x84	RGB3_DIM	7	Reserved	0	RW	Keep default value
		6:5	ISINK3_DIM_MODE	11	RW	ISINK3 Mode Select 00 = PWM Mode 01 = Breath Mode 1X = Register Mode
		4:0	ISINK3_DIM_DUTY	00000	RW	ISINK3 PWM Mode

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						Dimming Duty = (N+1)/32 N = 0 to 31
0x85	RGB_EN	7	ISINK1_DIM_EN	0	RW	ISINK1 Current Sink Enable 0: Disable 1: Enable
		6	ISINK2_DIM_EN	0	RW	ISINK2 Current Sink Enable 0: Disable 1: Enable
		5	ISINK3_DIM_EN	0	RW	ISINK3 Current Sink Enable 0: Disable 1: Enable
		4	ISINK4_CHRIND_EN	0	RW	ISINK4_CHRIND Current Sink Enable 0: Disable 1: Enable
		3	ISINK1_SFSTR_EN	1	RW	ISINK1 Soft Start Function Enable control 0: Disable RGB1 Soft Start Function 1: Enable RGB1 Soft Start Function
		2	ISINK2_SFSTR_EN	1	RW	ISINK2 Soft Start Function Enable control 0: Disable RGB2 Soft Start Function 1: Enable RGB2 Soft Start Function
		1	ISINK3_SFSTR_EN	1	RW	ISINK3 Soft Start Function Enable control 0: Disable RGB3 Soft Start Function 1: Enable RGB3 Soft Start Function
		0	ISINK4_CHRIND_SFSTR_EN	1	RW	ISINK4_CHRIND Soft Start Function Enable control 0: Disable RGB4 Soft Start Function 1: Enable RGB4 Soft Start Function
0x86	RGB1_ISNK	7:6	ISINK1_SFSTR_TC	00	RW	ISINK1 Soft Start Time Step Control 00 = 0.5µs 01 = 1µs 10 = 1.5µs 11 = 2µs
		5:3	ISINK1_DIM_FSEL	001	RW	ISINK1 PWM Mode Dimming Frequency Select 000 = 0.1Hz 001 = 0.2Hz 010 = 0.5Hz 011 = 1Hz 100 = 2Hz 101 = 5Hz 110 = 200Hz 111 = 1kHz

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		2:0	ISINK1_CUR_SEL	010	RW	ISINK1 Current Level Select 000 = 0mA 001 = 4mA 010 = 8mA 011 = 12mA 100 = 16mA 101 = 20mA 110 = 24mA 111 = 24mA
0x87	RGB2_ISNK	7:6	ISINK2_SFSTR_TC	00	RW	ISINK2 Soft Start Time Step Control 00 = 0.5µs 01 = 1µs 10 = 1.5µs 11 = 2µs
		5:3	ISINK2_DIM_FSEL	001	RW	ISINK2 PWM Mode Dimming Frequency Select 000 = 0.1Hz 001 = 0.2Hz 010 = 0.5Hz 011 = 1Hz 100 = 2Hz 101 = 5Hz 110 = 200Hz 111 = 1kHz
		2:0	ISINK2_CUR_SEL	010	RW	ISINK2 Current Level Select 000 = 0mA 001 = 4mA 010 = 8mA 011 = 12mA 100 = 16mA 101 = 20mA 110 = 24mA 111 = 24mA
0x88	RGB3_ISNK	7:6	ISINK3_SFSTR_TC	00	RW	ISINK3 Soft Start Time Step Control 00 = 0.5µs 01 = 1µs 10 = 1.5µs 11 = 2µs
		5:3	ISINK3_DIM_FSEL	001	RW	ISINK3 PWM Mode Dimming Frequency Select 000 = 0.1Hz 001 = 0.2Hz 010 = 0.5Hz 011 = 1Hz 100 = 2Hz 101 = 5Hz 110 = 200Hz 111 = 1kHz
		2:0	ISINK3_CUR_SEL	010	RW	ISINK3 Current Level Select 000 = 0mA 001 = 4mA 010 = 8mA 011 = 12mA 100 = 16mA

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						101 = 20mA 110 = 24mA 111 = 24mA
0x89	RGB1_Tr	7:4	ISINK1_BREATH_Tr1_SEL	0101	RW	ISINK1 Breath Mode First Rising Time Select Duty: 0% ~ 30% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 0101 = 1.125s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK1_BREATH_Tr2_SEL	0010	RW	ISINK1 Breath Mode Second Rising Time Select Duty: 31% ~ 100% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
0x8A	RGB1_Tf	7:4	ISINK1_BREATH_Tf1_SEL	0010	RW	ISINK1 Breath Mode First Falling Time Select Duty: 100% ~ 31% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK1_BREATH_Tf2_SEL	0101	RW	ISINK1 Breath Mode Second Falling Time Select Duty: 30% ~ 0% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 0101 = 1.125s ... 1111 = 3.125s 16 Steps, 0.2s/step
0x8B	RGB1_TON_TOFF	7:4	ISINK1_BREATH_TON_SEL	0001	RW	ISINK1 Breath Mode On Time Select 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK1_BREATH_TOFF_SEL	0001	RW	ISINK1 Breath Mode Off Time Select 0000 = 0.25s 0001 = 0.65s 0010 = 1.05s ... 1111 = 6.25s 16 Steps, 0.4s/step

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x8C	RGB2_Tr	7:4	ISINK2_BREATH_Tr1_SEL	0101	RW	ISINK2 Breath Mode First Rising Time Select Duty: 0% ~ 30% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK2_BREATH_Tr2_SEL	0010	RW	ISINK2 Breath Mode Second Rising Time Select Duty: 31 % ~ 100 % 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
0x8D	RGB2_Tf	7:4	ISINK2_BREATH_Tf1_SEL	0010	RW	ISINK2 Breath Mode First Falling Time Select Duty: 100% ~ 31% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK2_BREATH_Tf2_SEL	0101	RW	ISINK2 Breath Mode Second Falling Time Select Duty: 30% ~ 0% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 0101 = 1.125s ... 1111 = 3.125s 16 Steps, 0.2s/step
0x8E	RGB2_TON_TOFF	7:4	ISINK2_BREATH_TON_SEL	0001	RW	ISINK2 Breath Mode On Time Select 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK2_BREATH_TOFF_SEL	0001	RW	ISINK2 Breath Mode Off Time Select 0000 = 0.25s 0001 = 0.65s 0010 = 1.05s ... 1111 = 6.25s 16 Steps, 0.4s/step
0x8F	RGB3_Tr	7:4	ISINK3_BREATH_TON_SEL	0101	RW	ISINK3 Breath Mode First Rising Time Select Duty: 0% ~ 30% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						... 0101 = 1.125s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK3_BREATH_TOFF_SEL	0010	RW	ISINK3 Breath Mode Second Rising Time Select Duty: 31% ~ 100% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
0x90	RGB3_Tf	7:4	ISINK3_BREATH_Tf1_SEL	0010	RW	ISINK3 Breath Mode First Falling Time Select Duty: 100% ~ 31% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK3_BREATH_Tf2_SEL	0101	RW	ISINK3 Breath Mode Second Falling Time Select Duty: 30% ~ 0% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 0101 = 1.125s ... 1111 = 3.125s 16 Steps, 0.2s/step
0x91	RGB3_TON_TOFF	7:4	ISINK3_BREATH_TON_SEL	0001	RW	ISINK3 Breath Mode On Time Select 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK3_BREATH_TOFF_SEL	0001	RW	ISINK3 Breath Mode Off Time Select 0000 = 0.25s 0001 = 0.65s 0010 = 1.05s ... 1111 = 6.25s 16 Steps, 0.4s/step
0x92	RGB_CHRIND_DIM	7	ISINK4_CHRIND_EN_SEL	0	RW	ISINK4_CHRIND CHG_VIN power good Indicator Control Mode Select 0 = Auto Mode(CHG_VIN power good Indicator) 1 = Software Mode
		6:5	ISINK4_CHRIND_DIM_MODE	11	RW	ISINK4_CHRIND Mode Select 00 = PWM Mode

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						01 = Breath Mode 1X = Register Mode
		4:0	ISINK4_CHRIND_DIM_DUTY	00000	RW	ISINK4_CHRIND PWM Mode Dimming Duty = (N+1)/32 N = 0 ~ 31
0x93	RGB_CHRIND_Ctrl	7	ISINK4_CHRIND_HCUR_EN	0	RW	ISINK4_CHRIND Current high/low level selection 0: Lower current level group 1: Higher current level group
		6:5	ISINK4_CHRIND_SFSTR_TC	00	RW	ISINK4_CHRIND Soft Start Time Step Control (Total 32 Steps) 00 = 0.5μs 01 = 1μs 10 = 1.5μs 11 = 2μs
		4:2	ISINK4_CHRIND_DIM_FSEL	001	RW	ISINK4_CHRIND PWM Mode Dimming Frequency Select 000 = 0.1Hz 001 = 0.2Hz 010 = 0.5Hz 011 = 1Hz 100 = 2Hz 101 = 5Hz 110 = 200Hz 111 = 1kHz
		1:0	ISINK4_CHRIND_CUR_SEL	11	RW	ISINK4_CHRIND Current Level Select If REG_PMU 0x93[7]: ISINK4_CHRIND_HCUR_EN = 1'b0 00 = 1mA 01 = 2mA 10 = 4mA 11 = 6mA (default) If REG_PMU 0x93[7]: ISINK4_CHRIND_HCUR_EN = 1'b1 00 = 8mA 01 = 12mA 10 = 16mA 11 = 20mA
0x94	RGB_CHRIND_Tr	7:4	ISINK4_CHRIND_BREATH_Tr1_SEL	0101	RW	ISINK4_CHRIND Breath Mode First Rising Time Select Duty: 0% ~ 30% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 0101 = 1.125s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK4_CHRIND_BREATH_Tr2_SEL	0010	RW	ISINK4_CHRIND Breath Mode Second Rising Time Select

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						Duty: 31% ~ 100% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
0x95	RGB_CHRIND_Tf	7:4	ISINK4_CHRIND_BREATH_Tf1_SEL	0010	RW	ISINK4_CHRIND Breath Mode First Falling Time Select Duty: 100% ~ 31% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK4_CHRIND_BREATH_Tf2_SEL	0101	RW	ISINK4_CHRIND Breath Mode Second Falling Time Select Duty: 30% ~ 0% 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 0101 = 1.125s ... 1111 = 3.125s 16 Steps, 0.2s/step
0x96	RGB_CHRIND_TON_TOFF	7:4	ISINK4_CHRIND_BREATH_TON_SEL	0001	RW	ISINK4_CHRIND Breath Mode On Time Select 0000 = 0.125s 0001 = 0.325s 0010 = 0.525s ... 1111 = 3.125s 16 Steps, 0.2s/step
		3:0	ISINK4_CHRIND_BREATH_TOFF_SEL	0001	RW	ISINK4_CHRIND Breath Mode Off Time Select 0000 = 0.25s 0001 = 0.65s 0010 = 1.05s ... 1111 = 6.25s 16 Steps, 0.4s/step
0x97	RGB_OPEN_SHORT_EN	7	ISINK4_CHRIND_OPEN_EN	0	RW	ISINK4_CHRIND Open Protection Enable 0: Disable 1: Enable
		6	ISINK3_OPEN_EN	0	RW	ISINK3 Open Protection Enable 0: Disable 1: Enable
		5	ISINK2_OPEN_EN	0	RW	ISINK2 Open Protection Enable 0: Disable 1: Enable
		4	ISINK1_OPEN_EN	0	RW	ISINK1 Open Protection Enable 0: Disable 1: Enable

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		3	ISINK4_CHRIND _SHORT_EN	0	RW	ISINK4_CHRIND Short Protection Enable 0: Disable 1: Enable
		2	ISINK3_SHORT_EN	0	RW	ISINK3 Short Protection Enable 0: Disable 1: Enable
		1	ISINK2_SHORT_EN	0	RW	ISINK2 Short Protection Enable 0: Disable 1: Enable
		0	ISINK1_SHORT_EN	0	RW	ISINK1 Short Protection Enable 0: Disable 1: Enable
0x9F	Reserved	7:0	Reserved	00000000	RW	Keep default value
0xA0	BL_EN	7	bled_ext_en	0	R/W	BackLight external control enable. 0 = I²C control 1 = external pin control
		6	bled_en	0	R/W	Back Light Enable 0 = Off 1 = Enable Back Light
		5	bled_1ch_en	0	R/W	Channel 1 0 = Disable 1 = Enable
		4	bled_2ch_en	0	R/W	Channel 2 0 = Disable 1 = Enable
		3	bled_3ch_en	0	R/W	Channel 3 0 = Disable 1 = Enable
		2	bled_4ch_en	0	R/W	Channel 4 0 = Disable 1 = Enable
		1	bled_code	1	RW	BLED Mapng Code 0 = Exponential 1 = Linear
		0	bled_config	0	RW	BLED PWM Configuration 0 = Active High 1 = Active Low
0xA1	BL_BST_CTRL	7	BL_OVP_EN	1	RW	Backlight OVP shutdown enable 0: OVP Shutdown 1: Report only, Backlight Boost Output > OVP Threshold
		6:5	BL_OVP	11	RW	BLED OVP 00: 17V 01: 21V 10: 25V 11: 29V
		4	Reserved	0	RW	Keep default value
		3	BL_OC_EN	1	RW	Backlight OC shutdown enable 0: OC Limit 1: Report only, Backlight Boost switch current > Current Limit Threshold

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		2:1	BL_OC	10	RW	BLED OC Current Limit 00: 900mA 01: 1200mA 10: 1500mA 11: 1800mA
		0	bled_swfreq	1	RW	BLED Switching frequency 0: 500kHz 1: 1.0MHz
0xA2	BL_PWM	7	bled_pwm	0	RW	PWM Enable 0 = PWM Ignored 1 = PWM Enable
		6:5	PWM_deglitch	01	RW	PWM Glitch Filter Time Setting 00: No filter 01: 100ns 10: 160ns 11: 200ns
		4:3	PWM_fsample	01	RW	PWM Sampling Frequency: 00: 1MHz 01: 4MHz 1X: 24MHz
		2	PWM_HYS_EN	1	RW	PWM Input Hysteresis 0: Disable 1: Enable
		1:0	PWM_HYS	00	RW	PWM Input Hysteresis 00: 1bit 01: 2bit 10: 4bit 11: 6bit
0xA3	BL_CTRL	7:4	bled_ramptime	0011	RW	BLED ramp-up/down time 0000: 0s 0001: 500µs 0010: 750µs 0011: 1ms 0100: 2ms 0101: 5ms 0110: 10ms 0111: 20ms 1000: 50ms 1001: 100ms 1010: 250ms 1011: 800ms 1100: 1s 1101: 2s 1110: 4s 1111: 8s
		3:0	Reserved	0000	RW	Keep default value
0xA4	BL_DIM2	7:3	Reserved	00000	RW	Keep default value
		2:0	bled_dim	111	RW	bled brightness control of 11 bit LSB's
0xA5	BL_DIM1	7:0	bled_dim	11111111	RW	bled brightness control of 11 bit MSB's . As 0xA5 modify, 0XA4 & 0xA5 data will be update for IC at same time. Suggest that first modify 0xA4, then modify 0xA5

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0xA6	BL_AFH	7:0	bled_autofreqhigh	00000000	RW	When bled_dim code is equal to or less than the bled_autofreqhigh, the backlight boost switching frequency is set to 500kHz.
0xA7	BL_FL	7:6	bled_flash_mode	00	RW	Backlight Torch/Strobe Mode Control 00: Backlight Strobe/Torch Disable. 01: Backlight Strobe Enable. 10: Backlight Torch Enable 11: Backlight Torch Enable When backlight Torch/Strobe Mode in 01/10/11, PWM control is disable and backlight current set to Bled_Strobe_Current or Bled_Torch_Current. After Strobe Function Timeout, bled_flash_mode set to 00 and return to backlight normal operation.
		5:3	bled_flash_ramp	001	RW	Backlight Torch/Strobe Function ramp up/down time setting 000 : 0μs 001 : 500μs 010 : 750μs 011 : 1ms 100 : 2ms 101 : 5ms
		2:0	Reserved	000	RW	Keep default value
0xA8	BL_FL_TO	7	bled_Strobe_timeout_en	1	RW	Backlight Strobe Function timeout Enable 0: Disable 1: Enable
		6:0	bled_Strobe_timeout	0001100	RW	Backlight Strobe Function timeout setting 7 bit programmable from 16ms to 2048ms in 16ms/code 0000000 = 16ms 0000001 = 32ms 0000010 = 48ms 0000011 = 64ms 0000100 = 80ms ... 0001100 = 208ms ... 1111111 = 2048ms
0xA9	BL_TOR_CTRL	7:0	bled_torch_current	10000000	RW	Backlight torch brightness control single channel 256 steps, 8bit MSB of Backlight 00000000 = disable 00000001 = 0.1172mA 00000010 = 0.2345mA

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						… 10000000 = 15.0073mA … 11111111 = 30mA
0xAA	BL_STRB_CTRL	7:0	bled_strobe_current	11111111	RW	Backlight strobe brightness control single channel 256 steps, 8bit MSB of Backlight 00000000 = disable 00000001 = 0.1172mA 00000010 = 0.2345mA … 10000000 = 15.0073mA … 11111111 = 30mA
0xB0	DB_CTRL1	7	db_periodic_mode	0	RW	DB periodic mode 0 = always on if DB is enable 1 = DB periodic mode
		6	db_freq_pm	0	RW	0 = 20 Hz 1= 33Hz when the register db_periodic_mode = 1
		5	db_single_pin	0	RW	Take effect only when the register db_ext_en = 1 0: VPOS & VNEG are controlled by DB_ENP & DB_ENN separately 1: VPOS & VNEG are controlled by DB_ENP
		4	db_periodic_fix	0	RW	Enable this bit to prevent from voltage drop when DB is restarted
		3	db_scp_hiccup	0	RW	DB VPOS / VNEG SCP HICCUP enable 0: Disable VPOS / VNEG SCP hiccup 1: Enable VPOS / VNEG SCP hiccup
		2:1	Reserved	00	RW	Keep default value
		0	db_ext_en	0	R/W	DB external control enable 0 = I^{2}C control 1 = external pin control
0xB1	DB_CTRL2	7	dsv_scp_hiccup	0	RW	DSV VPOS/VNEG SCP HICCUP Enable 0: Disable VPOS/VNEG SCP Hiccup 1: Enable VPOS/VNEG SCP Hiccup
		6	db_vpos_en	0	RW	DB VPOS enable 0 = disable 1 = enable
		5	db_vpos_disc	0	RW	DB VPOS discharge enable 0 = floating 1 = discharge only function when VPOS is disable
		4	db_vpos_20ms	1	RW	DB VPOS discharge 20ms

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						when shutdown 0 = disable 1 = enable
		3	db_vneg_en	0	RW	DB VNEG enable 0 = disable 1 = enable
		2	db_vneg_disc	0	RW	DB VNEG discharge enable 0 = floating 1 = discharge only function when VNEG is disable
		1	db_vneg_20ms	1	RW	DB VNEG discharge 20ms when shutdown 0 = disable 1 = enable
		0	db_startup	0	RW	DB startup mode 0 = close loop, waiting 80% 1 = open loop, go after soft-start dimming
0xB2	DB_VBST	7:6	db_delay	01	RW	DB delay time between endpoint of VPOS ramp up and starting point of VNEG ramp down 00 = no constraint 01 = 0ms 10 = 1ms 11 = 4ms
		5:0	db_vbst	100010	RW	Vbst Voltage [000000] = 4V [010100] = 5V [100010] = 5.7V [101000] = 6V [101100] = 6.2V (0.05V per step, for code > [101100] will also equal to 6.2V)
0xB3	DB_VPOS	7:6	db_vpos_slew	01	RW	DB_POSVOUT slew rate 00: 8.54V/ms 01: 5.84V/ms 10: 4.83V/ms 11: 3.00V/ms
		5:0	db_vpos	011110	RW	DB_POSVOUT voltage 000000: 4V 010100: 5V 011110: 5.5V 101000: 6V ... 111111 : 6V (0.05V/step, for code > “101000” will also equal to 6V)
0xB4	DB_VNEG	7:6	db_vneg_slew	01	RW	DB_NEGVOUT slew rate 00: -10.09V/ms 01: -6.31V/ms 10: -5.05V/ms 11: -3.15V/ms
		5:0	db_vneg	011110	RW	DB_NEGVOUT voltage 000000: -4V 010100: -5V

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						011110: -5.5V 101000: -6V ... 111111 : -6V (0.05V/step, for code > "101000" will also equal to -6V)
0xC0	CHG_IRQ1	7	PWR_RDY_EVT	0	R	Power ready detection result: Input power is good, UVLO < VIN < VOVP & VIN > BATS + VSLP 0: No operation 1: Event occurs
		6	CHG_MIVR_EVT	0	R	Charger warning. Input voltage MIVR loop active. 0: No operation 1: Event occurs
		5	CHG_AICR_EVT	0	R	Charger warning. Input current AICR loop active. 0: No operation 1: Event occurs
		4	CHG_TREG_EVT	0	R	Charger warning. Thermal regulation loop active. 0: No operation 1: Event occurs
		3:0	Reserved	0000	R	Reserved
0xC1	CHG_IRQ2	7	CHG_VINOVPCHG_EVT	0	R	CHG_VIN over 14.5V voltage protection fault. It will forbid charger operation. 0: No operation 1: Event occurs
		6	CHG_VBATOV_EVT	0	R	Charger fault. Battery OVP fault 0: No operation 1: Event occurs
		5	CHG_VSYSOV_EVT	0	R	Charger fault. System OVP fault 0: No operation 1: Event occurs
		4	CHG_VSYSUV_EVT	0	R	Charger fault. System UVP fault 0: No operation 1: Event occurs
		3	FL-CHG_VINOVP_EVT	0	R	CHG_VIN over 5.6V voltage protection fault. It will forbid strobe operation. 0: No operation 1: Event occurs
		2:0	Reserved	000	R	Reserved
0xC2	CHG_IRQ3	7	TS_BAT_HOT_EVT	0	R	BAT temperature fault 0: No operation 1: Event occurs
		6	TS_BAT_WARM_EVT	0	R	BAT temperature fault 0: No operation 1: Event occurs
		5	TS_BAT_COOL_EVT	0	R	BAT temperature fault 0: No operation 1: Event occurs

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		4	TS_BAT_COLD_EVT	0	R	BAT temperature fault 0: No operation 1: Event occurs
		3:0	Reserved	0000	R	Reserved
0xC3	CHG_IRQ4	7	OTPI_EVT	0	RC	Thermal shutdown fault 0: No operation 1: Event occurs
		6	CHG_RVPI_EVT	0	RC	Charger reverse protection fault 0: No event occurs 1: Event occurs
		5	CHG_ADPBADI_EVT	0	RC	Charger bad adapter fault 0: No event occurs 1: Event occurs
		4	CHG_BATABSI_EVT	0	RC	Battery absence fault 0: No event occurs 1: Event occurs
		3	CHG_TMRI_EVT	0	RC	Charger timer time-out fault 0: No event occurs 1: Event occurs
		2:0	Reserved	000	RC	Reserved
0xC4	CHG_IRQ5	7	CHG_IEOCI_EVT	0	RC	Charging current is lower than EOC current event occurs 0: No event occurs 1: Event occurs
		6	CHG_TERMI_EVT	0	RC	Charge termination event 0: No event occurs 1: Event occurs
		5	CHG_RECHGI_EVT	0	RC	Re-Charge event occurs. 0: No event occurs 1: Event occurs
		4	SSFINISHI_EVT	0	RC	Charger or Boost soft-start finishes event 0: No event occurs 1: Event occurs
		3	WDTMRI_EVT	0	RC	Watch dog timer timeout fault 0: No event occurs 1: Event occurs
		2	CHGDET_DONEI_EVT	0	RC	Charger type detection done event 0: No event occurs 1: Event occurs
		1	CHG_ICHGMeasI_EVT	0	RC	ICHG measurement function done event 0: No event occurs 1: Event occurs
		0	CHG_AICLMeasI_EVT	0	RC	AICL measurement function done event 0: No event occurs 1: Event occurs
0xC5	CHG_IRQ6	7	BST_OLPI_EVT	0	RC	Boost overload protection event 0: No event occurs 1: Event occurs
		6	BST_MIDOVI_EVT	0	RC	Boost CHG_VMID OVP fault event 0: No event occurs

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						1: Event occurs
		5	BST_BATUVI_EVT	0	RC	Boost low voltage input fault event 0: No event occurs 1: Event occurs
		4:2	Reserved	000	RW	Reserved
		1	PUMPX_DONEI_EVT	0	RC	MTK pump express function done event 0: No event occurs 1: Event occurs
		0	ADC_DONEI	0	RC	ADC measurement done event 0: No event occurs 1: Event occurs

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0xC6	DPDM IRQ	7	DCDTI_EVT	0	RC	Data contact detection event 0: Data Contact Detection timeout is not detected 1: Data Contact Detection timeout is detected when DCDT goes from 0 to 1
		6	CHGDETI_EVT	0	RC	Output of USB charger detection. The bit will be set to 1 if COMN > VDAT_REF & COMN < VLGC 0: COMN < VDAT_REF or COMN > VLGC (charger port is not detected) 1: COMN > VDAT_REF & COMN < VLGC (charger port is detected) when CHGDET goes from 0 to 1
		5	HVDCP DET_EVT	0	RC	0: HVDCP not detected by DCP's pulling D- to GND 1: HVDCP detected by DCP's pulling D- to GND
		4:2	Reserved	0	RC	Reserved
		1	Detach_I_EVT	0	RC	VBUS detach, when VBUSPG_D goes from 1 to 0 0: No event occurs 1: Event occurs
		0	Attach_I_EVT	0	RC	VBUS attach, When DCP STD (Reg0x22[2]) goes from 0 to 1 or When CDP (Reg0x22[1]) goes from 0 to 1 or When SDP (Reg0x22[0]) goes from 0 to 1 0: No event occurs 1: Event occurs
0xC8	OVPCTRL_IRQ	7	OVPCTRL_OVP_EVT	0	R	OVPCTRL VBUS over-voltage protection fault (Rising/Falling trigger) 0: No operation 1: Event occurs
		6	OVPCTRL_OVP_D_EVT	0	R	OVPCTRL VBUS over-voltage protection fault with 128μs deglitch time (Rising/Falling trigger) 0: No operation 1: Event occurs
		5	OVPCTRL_UVP_EVT	0	R	OVPCTRL VBUS under-voltage protection fault (Rising/Falling trigger) 0: No operation 1: Event occurs
		4	OVPCTRL_UVP_D_EVT	0	R	OVPCTRL VBUS under-voltage protection fault with 128μs deglitch time (Rising/Falling trigger) 0: No operation 1: Event occurs

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		3	OVPCTRL_SWON_EVT	0	R	OVPCTRL MOS is turned on (Rising/Falling trigger) 0: No operation 1: Event occurs
		2:0	Reserved	000	R	Reserved
0xC9	FLED_IRQ1	7	FLED1_SHORT_EVT	0	RC	Report whether the event of FLED1 short-circuit occurs. 0: No event occurs. 1: Event ever occurs.
		6	FLED2_SHORT_EVT	0	RC	Report whether the event of FLED2 short-circuit occurs. 0: No event occurs. 1: Event ever occurs.
		5:4	Reserved	00	RC	Keep default value
		3	FLED_LVF_EVT	0	RC	Report whether the event of FLED low VF occurs. 0: No event occurs. 1: Event ever occurs.
		2	FLED_TX_EVT	0	RC	Report whether the event of FLED TXMask occurs. (If sENB_TX = 1'b1, this event will not interrupt) 0: No event occurs. 1: Event ever occurs.
		1	FLED_TORPIN_EVT	0	RC	Report whether the event of FLED torch pin occurs. 0: No event occurs. 1: Event ever occurs.
		0	FLED_STRBPIN_EVT	0	RC	Report whether the event of FLED strobe pin occurs. 0: No event occurs. 1: Event ever occurs.
0xCA	FLED_IRQ2	7:6	Reserved	00	RC	Keep default value
		5	FLED1_TOR_EVT	0	RC	Report whether the event of FLED1 torch occurs. 0: No event occurs. 1: Event ever occurs.
		4	FLED2_TOR_EVT	0	RC	Report whether the event of FLED2 torch occurs. 0: No event occurs. 1: Event ever occurs.
		3	FLED1_STRB_TO_EVT	0	RC	Report whether the event of FLED1 strobe timeout occurs. 0: No event occurs. 1: Event ever occurs.
		2	FLED2_STRB_TO_EVT	0	RC	Report whether the event of FLED2 strobe timeout occurs. 0: No event occurs. 1: Event ever occurs.
		1	FLED1_STRB_EVT	0	RC	Report whether the event of FLED1 strobe occurs. 0: No event occurs. 1: Event ever occurs.
		0	FLED2_STRB_EVT	0	RC	Report whether the event of FLED2 strobe occurs. 0: No event occurs.

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						1: Event ever occurs.
0xCB	BASE_IRQ	7	VDDA_UV_EVT	0	RC	Report whether the protection event of VDDA UVLO occurs. 0: No protection event occurs. 1: Protection event ever occurs.
		6	VDDA_OVP_EVT	0	RC	Report whether the protection event of VDDA OVP occurs. 0: No protection event occurs. 1: Protection event ever occurs.
		5	OTP_EVT	0	RC	Report whether the protection event of OTP ever occurs. 0: No protection event occurs. 1: Protection event ever occurs.
		4:0	Reserved	00000	RC	Keep default value
0xCC	LDO_IRQ	7	LDO_OC_EVT	0	RC	Report whether the event of LDO OC occurs. 0: No event occurs. 1: Event ever occurs.
		6:0	Reserved	0000000	RC	Keep default value
0xCD	RGB_IRQ	7	ISINK1_OPEN_EVT	0	RC	ISINK1 open-circuit LED Event 0: No protection event occurs. 1: Protection event ever occurs.
		6	ISINK2_OPEN_EVT	0	RC	ISINK2 open-circuit LED Event 0: No protection event occurs. 1: Protection event ever occurs.
		5	ISINK3_OPEN_EVT	0	RC	ISINK3 open-circuit LED Event 0: No protection event occurs. 1: Protection event ever occurs.
		4	ISINK4_OPEN_EVT	0	RC	ISINK4 open-circuit LED Event 0: No protection event occurs. 1: Protection event ever occurs.
		3	ISINK1_SHORT_EVT	0	RC	ISINK1 short-circuit LED Event 0: No protection event occurs. 1: Protection event ever occurs.
		2	ISINK2_SHORT_EVT	0	RC	ISINK2 short-circuit LED Event 0: No protection event

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						occurs. 1: Protection event ever occurs.
		1	ISINK3_SHORT_EVT	0	RC	ISINK3 short-circuit LED Event 0: No protection event occurs. 1: Protection event ever occurs.
		0	ISINK4_SHORT_EVT	0	RC	ISINK4 short-circuit LED Event 0: No protection event occurs. 1: Protection event ever occurs.
0xCE	BL_IRQ	7	bled_ovp_flag	0	R	Back Light OVP Flag 0: Normal 1: Fault
		6	bled_ocp_flag	0	RC	Back Light OCP flag 0: Normal 1: Fault
		5:0	Reserved	000000	RC	Keep default value
0xCF	DB_IRQ	7	db_vpos_scp_flag	0	RC	DB_POSVOUT short-circuit protection 0: Normal 1: Fault occurs
		6	db_vneg_scp_flag	0	RC	DB_NEGVOUT short-circuit protection 0: Normal 1: Fault occurs
		5	db_bst_ocp_flag	0	RC	DB_BSTVOUT over-current flag 0: Normal 1: Fault occurs
		4	db_vpos_ocp_flag	0	RC	DB_POSVOUT over-current flag 0: Normal 1: Fault occurs
		3	db_vneg_ocp_flag	0	RC	DB_NEGVOUT over-current flag 0: Normal 1: Fault occurs
		2:0	Reserved	000	RC	Keep default value
0xD0	CHG_STAT1	7	PWR_RDY_STAT	0	R	Power ready status bit 0: Input power is bad, CHG_VIN > VOVP or CHG_VIN < VUVLO or CHG_VIN < BATS + VSLP 1: Input power is good, UVLO < CHG_VIN < VOVP & CHG_VIN > BATS + VSLP
		6	CHG_MIVR_STAT	0	R	Charger warning. Input voltage MIVR loop active. 0: MIVR loop is not active 1: MIVR loop is active
		5	CHG_AICR_STAT	0	R	Charger warning. Input current AICR loop active. 0: AICR loop is not active 1: AICR loop is active

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		4	CHG_TREG_STAT	0	R	Charger warning. Thermal regulation loop active. 0: Thermal regulation loop is not active 1: Thermal regulation loop is active
		3:0	Reserved	0000	R	Reserved
0xD1	CHG_STAT2	7	CHG_VINOVPCHG_STAT	0	R	V_{CHG_VIN} over-voltage protection (when V_{CHG_VIN} > $V_{BUS_OVP_CHG}$) 0: V_{CHG_VIN} over-voltage does not occur 1: V_{CHG_VIN} over-voltage occurs
		6	CHG_VBATOV_STAT	0	R	Charger fault. Battery OVP. 0: Battery over-voltage does not occur 1: Battery over-voltage occurs
		5	CHG_VSYSOV_STAT	0	R	Charger fault. System OVP. 0: System over-voltage does not occur 1: System over-voltage occurs
		4	CHG_VSYSUV_STAT	0	R	Charger fault. System UVP. 0: System under-voltage does not occur 1: System under-voltage occurs
		3	FL-CHGVINOVP_STAT	0	R	V_{CHG_VIN} over 5.6V voltage protection status. It will forbid strobe operation. CHG_VIN OVP threshold voltage = $V_{OVP_STRB_FL}$ (Rising/falling = 5.6/5.3V (typ.)) 0: CHG_VIN over-voltage does not occur 1: CHG_VIN over-voltage occurs
		2:0	Reserved	000	R	Reserved
0xD2	CHG_STAT3	7	TS_BAT_HOT_STAT	0	R	BAT temperature status 0: Normal temperature 1: Temperature is hot
		6	TS_BAT_WARM_STAT	0	R	BAT temperature status 0: Normal temperature 1: Temperature is warm
		5	TS_BAT_COOL_STAT	0	R	BAT temperature status 0: Normal temperature 1: Temperature is cool
		4	TS_BAT_COLD_STAT	0	R	BAT temperature status 0: Normal temperature 1: Temperature is cold
		3:0	Reserved	0000	R	Reserved

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0xD3	CHG_STAT4	7	OTPI_STAT	0	R	Thermal shutdown status 0: No operation 1: Event occurs
		6	CHG_RVPI_STAT	0	R	Charger reverse protection status 0: No event occurs 1: Event occurs
		5	CHG_ADPBADI_STAT	0	R	Charger bad adapter status 0: No event occurs 1: Event occurs
		4	Reserved	0	R	Reserved
		3	CHG_TMRI_STAT	0	R	Charger timer time-out status 0: No event occurs 1: Event occurs
		2:0	Reserved	000	R	Reserved
0xD4	CHG_STAT5	7	CHG_IEOCI_STAT	0	R	Charging current is lower than EOC current ever occurs 0: No event occurs 1: Event occurs
		6	CHG_TERMI_STAT	0	R	Charge terminated event 0: No event occurs 1: Event occurs
		5	Reserved	0	R	Reserved
		4	SSFINISHI_STAT	0	R	Charger or Boost soft-start finishes event 0: No event occurs 1: Event occurs
		3	Reserved	0	R	Reserved
		2	CHGDET_DONEI_STAT	0	R	Charger type detection done event 0: No event occurs 1: Event occurs
		1:0	Reserved	00	R	Reserved
0xD5	CHG_STAT6	7	BST_OLPI_STAT	0	R	Boost overload protection event 0: No event occurs 1: Event occurs
		6	BST_MIDOVI_STAT	0	R	Boost CHG_VMID OVP fault event 0: No event occurs 1: Event occurs
		5	BST_BATUVI_STAT	0	R	Boost low voltage input fault event 0: No event occurs 1: Event occurs
		4:0	Reserved	000	R	Reserved
0xD6	DPDM_STAT	7	DCDTI_STAT	0	R	Data contact detection event 0: Data Contact Detection timeout is not detected 1: Data Contact Detection timeout is detected when DCDT goes from 0 to 1
		6	CHGDETI_STAT	0	R	Output of USB charger detection. The bit will be set to 1 if COMN > VDAT_REF & COMN <

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						VLGC 0: COMN < VDAT_REF or COMN > VLGC (charger port is not detected) 1: COMN > VDAT_REF & COMN < VLGC (charger port is detected) when CHGDET goes from 0 to 1
		5	HVDCP_DET_STAT	0	R	
		4:2	Reserved	000	R	Reserved
		1	Detach_I_STAT	0	R	VBUS detach, when VBUSPG_D goes from 1 to 0 0: No event occurs 1: Event occurs
		0	Attach_I_STAT	0	R	VBUS attach, When DCP STD (Reg0x22[2]) goes from 0 to 1 or When CDP (Reg0x22[1]) goes from 0 to 1 or When SDP (Reg0x22[0]) goes from 0 to 1 0: No event occurs 1: Event occurs
0xD8	OVPCTRL_STAT	7	OVPCTRL_OVP_STAT	0	R	OVPCTRL VBUS over-voltage protection 0: VBUS is not over-voltage 1: VBUS is over-voltage
		6	OVPCTRL_OVP_D_STAT	0	R	OVPCTRL VBUS over-voltage protection with 128μs deglitch time 0: VBUS is not over-voltage 1: VBUS is over-voltage with 128μs
		5	OVPCTRL_UVP_STAT	0	R	OVPCTRL VBUS under-voltage protection fault 0: VBUS is not under-voltage 1: VBUS is under-voltage
		4	OVPCTRL_UVP_D_STAT	0	R	OVPCTRL VBUS under-voltage protection fault with 128μs deglitch time 0: VBUS is not under-voltage 1: VBUS is under-voltage with 128μs
		3	OVPCTRL_SWON_STAT	0	R	OVPCTRL MOS is turned on 0: OVPCTRL MOS is off 1: OVPCTRL MOS is on
		2:0	Reserved	000	R	Reserved
0xD9	FLED_STAT1	7	FLED1_SHORT_STAT	0	R	FLED1 short-circuit Status 0: FLED1 short-circuit does not occur 1: FLED1 short-circuit occurred
		6	FLED2_SHORT_STAT	0	R	FLED2 short-circuit

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						Status 0: FLED2 short-circuit does not occur 1: FLED2 short-circuit occurred
		5:4	Reserved	00	R	Keep default value
		3	FLED_LVF_STAT	0	R	FLED low-VF Status 0: FLED low-VF does not occur 1: FLED low-VF occurred
		2	FLED_TX_STAT	0	R	FLED TXMask Status 0: FLED TXMask does not occur 1: FLED TXMask occurred
		1	FLED_TORPIN_STAT	0	R	FLED torch pin Status 0: FLED torch pin does not occur 1: FLED torch pin occurred
		0	FLED_STRBPIN_STAT	0	R	FLED strobe pin Status 0: FLED strobe pin does not occur 1: FLED strobe pin occurred
0xDA	FLED_STAT2	7:6	Reserved	00	R	Keep default value
		5	FLED1_TOR_STAT	0	R	FLED1 Torch mode Status 0: FLED1 Torch mode does not occur 1: FLED1 Torch mode occurred
		4	FLED2_TOR_STAT	0	R	FLED2 Torch mode Status 0: FLED2 Torch mode does not occur 1: FLED2 Torch mode occurred
		3	FLED1_STRB_TO_STAT	0	R	FLED1 Strobe Timeout Status 0: FLED1 Strobe Timeout does not occur 1: FLED1 Strobe Timeout occurred
		2	FLED2_STRB_TO_STAT	0	R	FLED2 Strobe Timeout Status 0: FLED2 Strobe Timeout does not occur 1: FLED2 Strobe Timeout occurred
		1	FLED1_STRB_STAT	0	R	FLED1 Strobe mode Status 0: PFLED1 Strobe does not occur 1: FLED1 Strobe occurred
		0	FLED2_STRB_STAT	0	R	FLED2 Strobe mode Status 0: FLED2 Strobe does not occur 1: FLED2 Strobe occurred
0xDB	BASE_STAT	7	VDDA_UV_STAT	0	R	VDDA UVLO Status 0: VDDA UVLO not occur 1: VDDA UVLO occurred

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		6	VDDA_OVP_STAT	0	R	VDDA OVP UVLO Status 0: VDDA OVP not occur 1: VDDA OVP occurred
		5	OTP_STAT	0	R	OTP Status 0:OTP not occur 1: OTP occurred
		4:0	Reserved	00000	R	Keep default value
0xDC	LDO_STAT	7	LDO_OC_STAT	0	R	General LDO OC Status 0: LDO OC not occur 1: LDO OC occurred
		6:0	Reserved	0000000	R	Keep default value
0xDD	RGB_STAT	7	ISINK1_OPEN_STAT	0	R	ISINK1 LED open-circuit State 0 = Normal 1 = Open-circuit LED
		6	ISINK2_OPEN_STAT	0	R	ISINK2 LED open-circuit State 0 = Normal 1 = Open-circuit LED
		5	ISINK3_OPEN_STAT	0	R	ISINK3 LED open-circuit State 0 = Normal 1 = Open-circuit LED
		4	ISINK4_OPEN_STAT	0	R	ISINK4 LED open-circuit State 0 = Normal 1 = Open-circuit LED
		3	ISINK1_SHORT_STAT	0	R	ISINK1 LED short-circuit State 0 = Normal 1 = Short-circuit LED
		2	ISINK2_SHORT_STAT	0	R	ISINK2 LED short-circuit State 0 = Normal 1 = Short-circuit LED
		1	ISINK3_SHORT_STAT	0	R	ISINK3 LED short-circuit State 0 = Normal 1 = Short-circuit LED
		0	ISINK4_SHORT_STAT	0	R	ISINK4 LED short-circuit State 0 = Normal 1 = Short-circuit LED
0xDE	BL_STAT	7	bled_ovp_STAT	0	R	Back Light OVP Status 0: Back Light OVP not occur 1: Back Light OVP occurred
		6	bled_ocp_STAT	0	R	Back Light's over-current status : 0: Back Light isn't over-current 1: Back Light is over-current
		5:0	Reserved	000000	R	Keep default value

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0xDF	DB_STAT	7	db_vpos_scp_STAT	0	R	DB_POSVOUT short-circuit protection status 0: DB_POSVOUT short-circuit protection does not occur 1: DB_POSVOUT short-circuit protection occurs
		6	db _vneg_scp_STAT	0	R	DB_NEGVOUT short-circuit protection status 0: DB_NEGVOUT short-circuit protection does not occur 1: DB_NEGVOUT short-circuit protection occurs
		5	db _bst_ocp_STAT	0	R	DB_BSTVOUT over-current protection status 0: DB_BSTVOUT over-current protection does not occur 1: DB_BSTVOUT over-current protection occurs
		4	db _vpos_ocp_STAT	0	R	DB_POSVOUT over-current protection status 0: DB_POSVOUT over-current protection does not occur 1: DB_POSVOUT over-current protection occurs
		3	db _vneg_ocp_STAT	0	R	DB_NEGVOUT over-current protection status 0: DB_NEGVOUT over-current protection does not occur 1: DB_NEGVOUT over-current protection occurs
		2:0	Reserved	000	R	Keep default value
0xE0	CHG_MASK1	7	PWR_RDYM	1	RW	Power ready interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		6	CHG_MIVRM	1	RW	Input voltage MIVR loop active interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		5	CHG_AICRM	1	RW	Input current AICR loop active interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		4	CHG_TREGM	1	RW	Thermal regulation loop active interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		3:0	Reserved	1111	RW	Reserved
0xE1	CHG_MASK2	7	CHG_VINOVPCHGM	1	RW	CHG_VIN over 14.5V voltage protection mask 0: Interrupt is not masked 1: Interrupt is masked
		6	CHG_VBATOVM	1	RW	Battery OVP interrupt mask 0: Interrupt is not masked 1: Interrupt is masked

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		5	CHG_VSYSOVM	1	RW	System OVP interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		4	CHG_VSYSUVM	1	RW	System UVP interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		3	FL-CHG_VINOVPM	1	RW	CHG_VIN over 5.6V voltage protection mask 0: Interrupt is not masked 1: Interrupt is masked
		2:0	Reserved	111	RW	Reserved
0xE2	CHG_MASK3	7	TS_BAT_HOTM	1	RW	BAT temperature status interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		6	TS_BAT_WARMM	1	RW	BAT temperature status interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		5	TS_BAT_COOLM	1	RW	BAT temperature status interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		4	TS_BAT_COLDM	1	RW	BAT temperature status interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		3:0	Reserved	1111	R	Reserved
0xE3	CHG_MASK4	7	OTPM	1	RW	Thermal shutdown fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		6	CHG_RVPM	1	RW	Charger reverse protection fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		5	CHG_ADPBADM	1	RW	Charger bad adapter fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		4	CHG_BATABSM	1	RW	Battery absence fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		3	CHG_TMRM	1	RW	Charger timer timeout fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		2:0	Reserved	111	RW	Reserved
0xE4	CHG_MASK5	7	CHG_IEOCM	1	RW	Charging current is lower than EOC current interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		6	CHG_TERMM	1	RW	Charge terminated event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		5	CHG_RECHGM	1	RW	Re-charge behavior interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		4	SSFINISHM	1	RW	Charger or Boost soft start finishes event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		3	WDTMRM	1	RW	Watch dog timer timeout fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		2	CHGDET_DONEM	1	RW	Charger type detection done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		1	CHG_ICHGMeasM	1	RW	ICHG measurement function done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		0	CHG_AICLMeasM	1	RW	AICL measurement function done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
0xE5	CHG_MASK6	7	BST_OLPM	1	RW	Boost overload protection event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		6	BST_MIDOVM	1	RW	Boost CHG_VMID OVP fault event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		5	BST_BATUVM	1	RW	Boost low voltage input fault event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		4:2	Reserved	111	RW	Reserved
		1	PUMPX_DONEM	1	RW	MTK pump express function done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		0	ADC_DONEM	1	RW	ADC measurement done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
0xE6	DPDM_MASK1	7	DCDTM	1	RW	Data contact detection event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		6	CHGDETM	1	RW	Output of USB charger detection interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		5	HVDCPDETM	1	RW	0: Interrupt is not masked 1: Interrupt is masked
		4:2	Reserved	111	RW	Reserved

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		1	Detach_M	1	RW	VBUS detach event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
		0	Attach_M	1	RW	VBUS attach event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
0xE8	OVPCTRL_ MASK	7	OVPCTRL_OVP_MASK	1	RW	OVPCTRL VBUS over-voltage protection fault mask 0: Interrupt is not masked 1: Interrupt is masked
		6	OVPCTRL_OVP_D_MASK	1	RW	OVPCTRL VBUS over-voltage protection fault with 128μs deglitch time mask 0: Interrupt is not masked 1: Interrupt is masked
		5	OVPCTRL_UVP_MASK	1	RW	OVPCTRL VBUS under-voltage protection fault mask 0: Interrupt is not masked 1: Interrupt is masked
		4	OVPCTRL_UVP_D_MASK	1	RW	OVPCTRL VBUS under-voltage protection fault with 128μs deglitch time mask 0: Interrupt is not masked 1: Interrupt is masked
		3	OVPCTRL_SWON_MASK	1	RW	OVPCTRL MOS is turned on mask 0: Interrupt is not masked 1: Interrupt is masked
		2:0	Reserved	111	RW	Reserved
0xE9	FLED_ MASK1	7	FLED1_SHORT_MASK	1	RW	FLED1 short-circuit mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		6	FLED2_SHORT_MASK	1	RW	FLED2 short-circuit mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		5:4	Reserved	11	RW	Keep default value
		3	FLED_LVF_MASK	1	RW	FLED low-VF mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		2	FLED_TX_MASK	1	RW	FLED TXMask mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		1	FLED_TORPIN_MASK	1	RW	FL_TORCH pin mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		0	FLED_STRBPIN_MASK	1	RW	FL_STROBE pin mask. 0: Interrupt is not masked. 1: Interrupt is masked.

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0xEA	FLED_MASK3	7:6	Reserved	11	RW	Keep default value
		5	FLED1_TOR_MASK	1	RW	FLED1 torch interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		4	FLED2_TOR_MASK	1	RW	FLED2 torch interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		3	FLED1_STRB_TO_MASK	1	RW	FLED1 strobe timeout interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		2	FLED2_STRB_TO_MASK	1	RW	FLED2 strobe timeout interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		1	FLED1_STRB_MASK	1	RW	FLED1 strobe interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		0	FLED2_STRB_MASK	1	RW	FLED2 strobe interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
0xEB	BASE_MASK	7	VDDA_UV_MASK	1	RW	VDDA UVLO interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		6	VDDA_OVP_MASK	1	RW	VDDA OVP interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		5	OTP_MASK	1	RW	OTP interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		4:0	Reserved	11111	RW	Keep default value
0xEC	LDO_MASK	7	LDO_OC_MASK	1	RW	General LDO OC interrupt mask. 0: Interrupt is not masked. 1: Interrupt is masked.
		6:0	Reserved	1111111	RW	Keep default value
0xED	RGB_MASK	7	ISINK1_OPEN_MASK	1	RW	RGB_ISINK1 LED open-circuit status mask 0: Not masked 1: Masked
		6	ISINK2_OPEN_MASK	1	RW	RGB_ISINK2 LED open-circuit status mask 0: Not masked 1: Masked

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		5	ISINK3_OPEN_MASK	1	RW	RGB_ISINK3 LED open-circuit status mask 0: Not masked 1: Masked
		4	ISINK4_OPEN_MASK	1	RW	RGB_ISINK4 LED open-circuit status mask 0: Not Masked 1: Masked
		3	ISINK1_SHORT_MASK	1	RW	ISINK1 LED short-circuit status mask 0: Not masked 1: Masked
		2	ISINK2_SHORT_MASK	1	RW	ISINK2 LED short-circuit status mask 0: Not masked 1: Masked
		1	ISINK3_SHORT_MASK	1	RW	ISINK3 LED short-circuit status mask 0: Not masked 1: Masked
		0	ISINK4_SHORT_MASK	1	RW	ISINK4 LED short-circuit status mask 0: Not masked 1: Masked
0xEE	BL_MASK	7	bled_ovp_MASK	1	RW	Backlight output OVP mask 0: Interrupt is not masked. 1: Interrupt is masked.
		6	bled_ocp_MASK	1	RW	Backlight over-current mask 0: Interrupt is not masked. 1: Interrupt is masked.
		5:0	Reserved	111111	RW	Keep default value
0xEF	DB_MASK	7	db_vpos_scp_MASK	1	RW	DB_POSVOUT short-circuit protection MASK 0: Interrupt is not masked. 1: Interrupt is masked.
		6	db_vneg_scp_MASK	1	RW	DB_NEGVOUT short-circuit protection MASK 0: Interrupt is not masked. 1: Interrupt is masked.
		5	db_bst_ocp_MASK	1	RW	DB_BSTVOUT over-current protection mask 0: Interrupt is not masked. 1: Interrupt is masked.
		4	db_vpos_ocp_MASK	1	RW	DB_POSVOUT over-current protection MASK 0: Interrupt is not masked. 1: Interrupt is masked.
		3	db_vneg_ocp_MASK	1	RW	DB_NEGVOUT over-current protection MASK 0: Interrupt is not masked. 1: Interrupt is masked.

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		2:0	Reserved	111	RW	Keep default value
0x00	VENDOR_ID	7:0	VID[7:0]	CF	R	A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.
0x01		7:0	VID[15:8]	29	R	
0x02	PRODUCT_ID	7:0	PID[7:0]	01	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC.
0x03		7:0	PID[15:8]	51	R	
0x04	DEVICE_ID	7:0	DID[7:0]	72	R	A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the TCPC.
0x05		7:0	DID[15:8]	30	R	
0x06	USBTYPEC_REV	7:0	USBTYPEC_REV	11	R	Version number assigned by USB-IF (Currently at Revision 1.1 – 0001 0001)
0x07		7:0	Reserved	00	R	
0x08	USBPD_REV_VER	7:0	USBPD_VER	10	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x09		7:0	USBPD_REV	30	R	0010 0000 – Revision 2.0 0011 0000 – Revision 3.0
0x0A	PD_INTERFACE_REV	7:0	PDIF_VER	10	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x0B		7:0	PDIF_REV	10	R	0010 0000 – Revision 2.0
0x10	ALERT	7	ALARM_VBUS_VOLTAGE_H	0	R	Not support
		6	TX_SUCCESS	0	RW	0b: Cleared 1b: Reset or SOP* message transmission successful.
		5	TX_DISCARD	0	RW	0b: Cleared 1b: Reset or SOP* message transmission not sent due to incoming receive message.
		4	TX_FAIL	0	RW	0b: Cleared 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.
		3	RX_HARD_RESET	0	RW	0b: Cleared 1b: Received Hard Reset message
		2	RX_SOP_MSG_STATUS	0	RW	0b: Cleared 1b: Receive status register changed
		1	POWER_STATUS	0	RW	0b: Cleared 1b: Port status changed
		0	CC_STATUS	0	RW	0b: Cleared 1b: CC status changed
0x11	ALERT	7	Reserved	0	R	
		6	Reserved	0	R	
		5	Reserved	0	R	
		4	Reserved	0	R	

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		3	VBUS_SINK_DISCNT	0	R	Not support
		2	RXBUF_OVFLOW	0	RW	0b: TCPC Rx buffer is functioning properly. 1b: TCPC Rx buffer has overflowed.
		1	FAULT	0	RW	0b: No Fault. 1b: A Fault has occurred. Read the FAULT_STATUS register.
		0	ALARM_VBUS_VOLTAGE_L	0	R	Not support
0x12	ALERT_MASK	7	M_ALARM_VBUS_VOLTAGE_H	1	RW	Not support
		6	M_TX_SUCCESS	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		5	M_TX_DISCARD	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		4	M_TX_FAIL	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		3	M_RX_HARD_RESET	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		2	M_RX_SOP_MSG_STATUS	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		1	M_POWER_STATUS	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		0	M_CC_STATUS	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
0x13	ALERT_MASK	7	Reserved	0	R	
		6	Reserved	0	R	
		5	Reserved	0	R	
		4	Reserved	0	R	
		3	M_VBUS_SINK_DISCNT	1	RW	Not support
		2	M_RXBUF_OVFLOW	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		1	M_FAULT	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		0	M_ALARM_VBUS_VOLTAGE_L	1	RW	Not support
0x14	POWER_STATUS_MASK	7	M_DBG_ACC_CONNECT	1	RW	Not support
		6	M_TCPC_INITIAL	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		5	M_SRC_HV	1	RW	Not support
		4	M_SRC_VBUS	1	RW	Not support
		3	M_VBUS_PRESENT_DETC	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		2	M_VBUS_PRESENT	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		1	M_VCONN_PRESENT	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		0	M_SINK_VBUS	1	RW	Not support

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x15	FAULT_STATUS_MASK	7	M_VCON_OV	0	RW	0b: Interrupt masked 1b: Interrupt unmasked
		6	M_FORCE_OFF_VBUS	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		5	M_AUTO_DISC_FAIL	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		4	M_FORCE_DISC_FAIL	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		3	M_VBUS_OC	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		2	M_VBUS_OV	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		1	M_VCON_OC	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
		0	M_I2C_ERROR	1	RW	0b: Interrupt masked 1b: Interrupt unmasked
0x18	CONFIG_STANDARD_OUTPUT	7	H_IMPEDENCE	0	R	Not support
		6	DBG_ACC_CONNECT_O	1	R	Not support
		5	AUDIO_ACC_CONNECT	1	R	Not support
		4	ACTIVE_CABLE_CONNECT	0	R	Not support
		3:2	MUX_CTRL	0	R	Not support
		1	CONNECT_PRESENT	0	R	Not support
		0	CONNECT_ORIENT	0	R	Not support
0x19	TCPC_CONTROL	7:5	Reserved	0	R	
		4	Reserved	0	R	
		3:2	I2C_CK_STRETCH	00	RW	Not support
		1	BIST_TEST_MODE	0	RW	0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.
		0	PLUG_ORIENT	0	RW	0b: When Vconn is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When Vconn is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled.

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						Required
0x1A	ROLE_CONTROL	7	Reserved	0	R	
		6	DRP	0	RW	0b: No DRP. Bits B3..0 determine Rp/Rd/Ra settings 1b: DRP
		5:4	RP_VALUE	0	RW	00b: Rp default 01b: Rp 1.5A 10b: Rp 3.0A 11b: Reserved
		3:2	CC2	10	RW	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6
		1:0	CC1	10	RW	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6
0x1B	FAULT_CONTROL	7	DIS_VCON_OV	0	RW	0b: Fault detection circuit enabled 1b: Fault detection circuit disabled
		6:5	Reserved	0	R	
		4	DIS_FORCE_OFF_VBUS	0	RW	Not support
		3	DIS_VBUS_DISC_FAULT_TIMER	0	RW	0b: VBUS Discharge Fault Detection Timer enabled 1b: VBUS Discharge Fault Detection Timer disabled
		2	DIS_VBUS_OC	0	RW	Not support
		1	DIS_VBUS_OV	0	RW	Not support
		0	DIS_VCON_OC	0	RW	0b: Fault detection circuit enabled 1b: Fault detection circuit disabled
0x1C	POWER_CONTROL	7	Reserved	0	R	
		6	VBUS_VOL_MONITOR	0	RW	Not support
		5	DIS_VOL_ALARM	0	RW	Not support
		4	AUTO_DISC_DISCNCT	1	RW	0b: The TCPC shall not automatically discharge VBUS based on VBUS voltage. 1b: The TCPC shall automatically discharge (default)
		3	BLEED_DISC	0	RW	0b: Disable bleed discharge (default) 1b: Enable bleed discharge of VBUS
		2	FORCE_DISC	0	RW	0b: Disable forced discharge (default) 1b: Enable forced

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						discharge of VBUS.
		1	VCONN_POWER_SPT	0	RW	0b: TCPC delivers at least 1W on VCONN 1b: TCPC delivers at least the power indicated in DEVICE_CAPABILITIES. VCONNPowerSupported
		0	EN_VCONN	0	RW	0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC Required
0x1D	CC_STATUS	7:6	Reserved	0	R	
		5	DRP_STATUS	0	R	0b: the TCPC has stopped toggling or (ROLE_CONTROL.DRP = 00) 1b: the TCPC is toggling
		4	DRP_RESULT	0	R	0b: the TCPC is presenting Rp 1b: the TCPC is presenting Rd

		3:2	CC2_STATUS	0	R	If (ROLE_CONTROL.CC2 = Rp) or (DrpResult = 0)
						00b: SRC.Open (Open, Rp)
						01b: SRC.Ra (below maximum vRa)
						10b: SRC.Rd (within the vRd range)
						11b: reserved
						
						If (ROLE_CONTROL.CC2 = Rd) or (DrpResult = 1)
						00b: SNK.Open (Below maximum vRa)
						01b: SNK.Default (Above minimum vRd-Connect)
						10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
						11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
						
						If ROLE_CONTROL.CC2 = Ra, this field is set to 00b
						If ROLE_CONTROL.CC2 = Open, this field is set to 00b
						
						This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVconn = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

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Address	Reg Name	Bit	Bit Name	Default	Type	Description

0x1D	CC_STATUS	1:0	CC1_STATUS	0	R	If (ROLE_CONTROL.CC1 = Rp) or (DrpResult = 0)
						00b: SRC.Open (Open, Rp)
						01b: SRC.Ra (below maximum vRa)
						10b: SRC.Rd (within the vRd range)
						11b: reserved
						
						If (ROLE_CONTROL.CC1 = Rd) or DrpResult = 1)
						00b: SNK.Open (Below maximum vRa)
						01b: SNK.Default (Above minimum vRd-Connect)
						10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A
						11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A
						
						If ROLE_CONTROL.CC1 = Ra, this field is set to 00b
						If ROLE_CONTROL.CC1 = Open, this field is set to 00b
						
						This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVconn = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x1E	POWER_STATUS	7	DBG_ACC_CONNECT	0	R	Not support
		6	TCPC_INITIAL	0	R	0b: The TCPC has completed initialization and all registers are valid 1b: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh
		5	SRC_HV	0	R	Not support
		4	SRC_VBUS	0	R	Not support
		3	VBUS_PRESENT_DETC	0	R	0b: VBUS Present Detection Disabled 1b: VBUS Present Detection Enabled (default)
		2	VBUS_PRESENT	0	R	0b: VBUS Disconnected 1b: VBUS Connected
		1	VCONN_PRESENT	0	R	0b: VCONN is not present 1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V
		0	SINK_VBUS	0	R	Not support
0x1F	FAULT_STATUS	7	VCON_OV	0	RW	0b: Not in an over-voltage protection state 1b: Over-voltage fault latched.
		6	FORCE_OFF_VBUS	0	RW	Not support
		5	AUTO_DISC_FAIL	0	RW	0b: No discharge failure 1b: Discharge commanded by the TCPM failed
		4	FORCE_DISC_FAIL	0	RW	0b: No discharge failure 1b: Discharge commanded by the TCPM failed.
		3	VBUS_OC	0	RW	Not support
		2	VBUS_OV	0	RW	Not support
		1	VCON_OC	0	RW	0b: No Fault detected 1b: Over current VCONN fault latched
		0	I2C_ERROR	0	RW	1. DisableVbusDetect while sourcing or sinking power over vbus enabled 2. TX_TRANSMIT with TX_BYTECOUNT < 2
0x23	COMMAND	7:0	COMMAND	0	R	0010_0010b: DisableVbusDetect 0011_0011b: EnableVbusDetect 1001_1001b: Start DRP Togging 1010_1010b: RXOneMore
0x24	DEVICE_CAPABILITIES_1L	7:5	ROLES_SUPPORT	110	R	000b: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						011b: Sink with accessory support (optional) 100b: DRP only 101b: Adapter or Cable (Ra) only 110b: Source, Sink, DRP, Adapter/Cable all supported 111b: Not valid
		4	ALL_SOP_SUPPORT	1	R	0b: All SOP* except SOP'_DBG/SOP"_DBG 1b: All SOP* messages are supported
		3	SOURCE_VCONN	1	R	0b: TCPC is not capable of switching VCONN 1b: TCPC is capable of switching VCONN
		2	CPB_SINK_VBUS	0	R	0b: TCPC is not capable controlling the sink path to the system load 1b: TCPC is capable of controlling the sink path to the system load
		1	SOURCE_HV_VBUS	0	R	0b: TCPC is not capable of controlling the source high voltage path to VBUS 1b: TCPC is capable of controlling the source high voltage path to VBUS
		0	SOURCE_VBUS	0	R	0b: TCPC is not capable of controlling the source path to VBUS 1b: TCPC is capable of controlling the source path to VBUS
0x25	DEVICE_CAPABILITIES_1H	7	Reserved	0	R	
		6	CPB_VBUS_OC	0	R	0b: VBUS OCP is not reported by the TCPC 1b: VBUS OCP is reported by the TCPC
		5	CPB_VBUS_OV	0	R	0b: VBUS OVP is not reported by the TCPC 1b: VBUS OVP is reported by the TCPC
		4	CPB_BLEED_DISC	1	R	0b: No Bleed Discharge implemented in TCPC 1b: Bleed Discharge is implemented in the TCPC
		3	CPB_FORCE_DISC	1	R	0b: No Force Discharge implemented in TCPC 1b: Force Discharge is implemented in the TCPC
		2	VBUS_MEASURE_ALARM	0	R	0b: No VBUS voltage measurement nor VBUS Alarms 1b: VBUS voltage measurement and VBUS Alarms

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
		1:0	SOURCE_RP_SUPPORT	10	R	00b: Rp default only 01b: Rp 1.5A and default 10b: Rp 3.0A, 1.5A, and default 11b: Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register
0x26	DEVICE_CAPABILITIES_2L	7	SINK_DISCONNECT_DET	0	R	0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default : Use POWER_STATUS.VbusPresent = 0b to indicate a Sink disconnect) 1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented
0x26	DEVICE_CAPABILITIES_2L	6	STOP_DISC_THD	0	R	0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented (default) 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented
		5:4	VBUS_VOL_ALARM_LSB	11	R	00: TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01: TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10: TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11: reserved
		3:1	VCONN_POWER	010	R	000b: 1.0W 001b: 1.5W

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
						010b: 2.0W 011b: 3W 100b: 4W 101b: 5W 110b: 6W 111b: External
		0	VCONN_OCF	1	R	0b: TCPC is not capable of detecting a Vconn fault 1b: TCPC is capable of detecting a Vconn fault
0x27	DEVICE_CAPABILITIES_2H	7:0	Reserved	0	R	
0x28	STANDARD_INPUT_CAPABILITIES	7:3	Reserved	0	R	
		2	VBUS_EXT_OVF	0	R	0b: Not present in TCPC 1b: Present in TCPC
		1	VBUS_EXT_OCF	0	R	0b: Not present in TCPC 1b: Present in TCPC
		0	FORCE_OFF_VBUS_IN	0	R	Not support
0x29	STANDARD_OUTPUT_CAPABILITIES	7	Reserved	0	R	
		6	CPB_DBG_ACC_IND	0	R	0b: Not present in TCPC 1b: Present in TCPC
		5	CPB_VBUS_PRESENT_MNT	0	R	0b: Not present in TCPC 1b: Present in TCPC
		4	CPB_AUDIO_ADT_ACC_IND	0	R	0b: Not present in TCPC 1b: Present in TCPC
		3	CPB_ACTIVE_CABLE_IND	0	R	0b: Not present in TCPC 1b: Present in TCPC
		2	CPB_MUX_CFG_CTRL	0	R	0b: Not present in TCPC 1b: Present in TCPC
		1	CPB_CONNECT_PRESENT	0	R	0b: Not present in TCPC 1b: Present in TCPC
		0	CPB_CONNECT_ORIENT	0	R	0b: Not present in TCPC 1b: Present in TCPC
0x2E	MESSAGE_HEADER_INFO	7:5	Reserved	0	R	
		4	CABLE_PLUG	0	RW	0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug
		3	DATA_ROLE	0	RW	0b: Sink 1b: Source
		2:1	USBPD_SPECREV	01	RW	00b: Revision 1.0 01b: Revision 2.0 10b – 11b: Reserved
		0	POWER_ROLE	0	RW	0b: Sink 1b: Source

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x2F	RECEIVE_DETECT	7	Reserved	0	R	
		6	EN_CABLE_RST	0	RW	0b: TCPC does not detect Cable Reset signaling (default) 1b: TCPC detects Cable Reset signaling
		5	EN_HARD_RST	0	RW	0b: TCPC does not detect Hard Reset signaling (default) 1b: TCPC detects Hard Reset signaling
		4	EN_SOP2DB	0	RW	0b: TCPC does not detect SOP_DBG'' message (default) 1b : TCPC detects SOP_DBG'' message
		3	EN_SOP1DB	0	RW	0b: TCPC does not detect SOP_DBG' message (default) 1b: TCPC detects SOP_DBG' message
		2	EN_SOP2	0	RW	0b: TCPC does not detect SOP'' message (default) 1b: TCPC detects SOP'' message
		1	EN_SOP1	0	RW	0b : TCPC does not detect SOP' message (default) 1b : TCPC detects SOP' message
		0	EN_SOP	0	RW	0b: TCPC does not detect SOP message (default) 1b: TCPC detects SOP message
0x30	RX_BYTE_COUNT	7:0	RX_BYTE_COUNT	0	RW	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register.
0x31	RX_BUF_FRAME_TYPE	7:3	Reserved	0	R	
		2:0	RX_FRAME_TYPE	0	R	Type of received frame 000b: Received SOP 001b: Received SOP' 010b: Received SOP" 011b: Received SOP_DBG' 100b: Received SOP_DBG'' 110b: Received Cable Reset All others are reserved.
0x32	RX_BUF_HEADER_BYTE_0	7:0	RX_HEAD_0	0	R	Byte 0 (bits 7..0) of message header
0x33	RX_BUF_HEADER_BYTE_1	7:0	RX_HEAD_1	0	R	Byte 1 (bits 15..8) of message header
0x34	RX_BUF_OBJ1_BYTE_0	7:0	RX_OBJ1_0	0	R	Byte 0 (bits 7..0) of 1st data object
0x35	RX_BUF_OBJ1_BYTE_1	7:0	RX_OBJ1_1	0	R	Byte 1 (bits 15..8) of 1st data object

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x36	RX_BUF_OBJ1_BYTE_2	7:0	RX_OBJ1_2	0	R	Byte 2 (bits 23..16) of 1st data object
0x37	RX_BUF_OBJ1_BYTE_3	7:0	RX_OBJ1_3	0	R	Byte 3 (bits 31..24) of 1st data object
0x38	RX_BUF_OBJ2_BYTE_0	7:0	RX_OBJ2_0	0	R	Byte 0 (bits 7..0) of 2st data object
0x39	RX_BUF_OBJ2_BYTE_1	7:0	RX_OBJ2_1	0	R	Byte 1 (bits 15..8) of 2st data object
0x3A	RX_BUF_OBJ2_BYTE_2	7:0	RX_OBJ2_2	0	R	Byte 2 (bits 23..16) of 2st data object
0x3B	RX_BUF_OBJ2_BYTE_3	7:0	RX_OBJ2_3	0	R	Byte 3 (bits 31..24) of 2st data object
0x3C	RX_BUF_OBJ3_BYTE_0	7:0	RX_OBJ3_0	0	R	Byte 0 (bits 7..0) of 3st data object
0x3D	RX_BUF_OBJ3_BYTE_1	7:0	RX_OBJ3_1	0	R	Byte 1 (bits 15..8) of 3st data object
0x3E	RX_BUF_OBJ3_BYTE_2	7:0	RX_OBJ3_2	0	R	Byte 2 (bits 23..16) of 3st data object
0x3F	RX_BUF_OBJ3_BYTE_3	7:0	RX_OBJ3_3	0	R	Byte 3 (bits 31..24) of 3st data object
0x40	RX_BUF_OBJ4_BYTE_0	7:0	RX_OBJ4_0	0	R	Byte 0 (bits 7..0) of 4st data object
0x41	RX_BUF_OBJ4_BYTE_1	7:0	RX_OBJ4_1	0	R	Byte 1 (bits 15..8) of 4st data object
0x42	RX_BUF_OBJ4_BYTE_2	7:0	RX_OBJ4_2	0	R	Byte 2 (bits 23..16) of 4st data object
0x43	RX_BUF_OBJ4_BYTE_3	7:0	RX_OBJ4_3	0	R	Byte 3 (bits 31..24) of 4st data object
0x44	RX_BUF_OBJ5_BYTE_0	7:0	RX_OBJ5_0	0	R	Byte 0 (bits 7..0) of 5st data object
0x45	RX_BUF_OBJ5_BYTE_1	7:0	RX_OBJ5_1	0	R	Byte 1 (bits 15..8) of 5st data object
0x46	RX_BUF_OBJ5_BYTE_2	7:0	RX_OBJ5_2	0	R	Byte 2 (bits 23..16) of 5st data object
0x47	RX_BUF_OBJ5_BYTE_3	7:0	RX_OBJ5_3	0	R	Byte 3 (bits 31..24) of 5st data object
0x48	RX_BUF_OBJ6_BYTE_0	7:0	RX_OBJ6_0	0	R	Byte 0 (bits 7..0) of 6st data object
0x49	RX_BUF_OBJ6_BYTE_1	7:0	RX_OBJ6_1	0	R	Byte 1 (bits 15..8) of 6st data object
0x4A	RX_BUF_OBJ6_BYTE_2	7:0	RX_OBJ6_2	0	R	Byte 2 (bits 23..16) of 6st data object
0x4B	RX_BUF_OBJ6_BYTE_3	7:0	RX_OBJ6_3	0	R	Byte 3 (bits 31..24) of 6st data object
0x4C	RX_BUF_OBJ7_BYTE_0	7:0	RX_OBJ7_0	0	R	Byte 0 (bits 7..0) of 7st data object
0x4D	RX_BUF_OBJ7_BYTE_1	7:0	RX_OBJ7_1	0	R	Byte 1 (bits 15..8) of 7st data object
0x4E	RX_BUF_OBJ7_BYTE_2	7:0	RX_OBJ7_2	0	R	Byte 2 (bits 23..16) of 7st data object
0x4F	RX_BUF_OBJ7_BYTE_3	7:0	RX_OBJ7_3	0	R	Byte 3 (bits 31..24) of 7st data object

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x50	TX_BUF_FRAME_TYPE	7:6	Reserved	0	R	
		5:4	TX_RETRY_CNT	0	RW	00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times
		3	Reserved	0	R	
		2:0	TX_FRAME_TYPE	0	RW	000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP" 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG" 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)
0x51	TX_BYTE_COUNT	7:0	TX_BYTE_COUNT	0	RW	The number of bytes the TCPM will write
0x52	TX_BUF_HEADER_BYTE_0	7:0	TX_HEAD_0	0	RW	Byte 0 (bits 7..0) of message header
0x53	TX_BUF_HEADER_BYTE_1	7:0	TX_HEAD_1	0	RW	Byte 1 (bits 15..8) of message header
0x54	TX_BUF_OBJ1_BYTE_0	7:0	TX_OBJ1_0	0	RW	Byte 0 (bits 7..0) of 1st data object
0x55	TX_BUF_OBJ1_BYTE_1	7:0	TX_OBJ1_1	0	RW	Byte 1 (bits 15..8) of 1st data object
0x56	TX_BUF_OBJ1_BYTE_2	7:0	TX_OBJ1_2	0	RW	Byte 2 (bits 23..16) of 1st data object
0x57	TX_BUF_OBJ1_BYTE_3	7:0	TX_OBJ1_3	0	RW	Byte 3 (bits 31..24) of 1st data object
0x58	TX_BUF_OBJ2_BYTE_0	7:0	TX_OBJ2_0	0	RW	Byte 0 (bits 7..0) of 2st data object
0x59	TX_BUF_OBJ2_BYTE_1	7:0	TX_OBJ2_1	0	RW	Byte 1 (bits 15..8) of 2st data object
0x5A	TX_BUF_OBJ2_BYTE_2	7:0	TX_OBJ2_2	0	RW	Byte 2 (bits 23..16) of 2st data object
0x5B	TX_BUF_OBJ2_BYTE_3	7:0	TX_OBJ2_3	0	RW	Byte 3 (bits 31..24) of 2st data object
0x5C	TX_BUF_OBJ3_BYTE_0	7:0	TX_OBJ3_0	0	RW	Byte 0 (bits 7..0) of 3st data object
0x5D	TX_BUF_OBJ3_BYTE_1	7:0	TX_OBJ3_1	0	RW	Byte 1 (bits 15..8) of 3st data object
0x5E	TX_BUF_OBJ3_BYTE_2	7:0	TX_OBJ3_2	0	RW	Byte 2 (bits 23..16) of 3st data object
0x5F	TX_BUF_OBJ3_BYTE_3	7:0	TX_OBJ3_3	0	RW	Byte 3 (bits 31..24) of 3st data object

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x60	TX_BUF_OBJ4_BYTE_0	7:0	TX_OBJ4_0	0	RW	Byte 0 (bits 7..0) of 4st data object
0x61	TX_BUF_OBJ4_BYTE_1	7:0	TX_OBJ4_1	0	RW	Byte 1 (bits 15..8) of 4st data object
0x62	TX_BUF_OBJ4_BYTE_2	7:0	TX_OBJ4_2	0	RW	Byte 2 (bits 23..16) of 4st data object
0x63	TX_BUF_OBJ4_BYTE_3	7:0	TX_OBJ4_3	0	RW	Byte 3 (bits 31..24) of 4st data object
0x64	TX_BUF_OBJ5_BYTE_0	7:0	TX_OBJ5_0	0	RW	Byte 0 (bits 7..0) of 5st data object
0x65	TX_BUF_OBJ5_BYTE_1	7:0	TX_OBJ5_1	0	RW	Byte 1 (bits 15..8) of 5st data object
0x66	TX_BUF_OBJ5_BYTE_2	7:0	TX_OBJ5_2	0	RW	Byte 2 (bits 23..16) of 5st data object
0x67	TX_BUF_OBJ5_BYTE_3	7:0	TX_OBJ5_3	0	RW	Byte 3 (bits 31..24) of 5st data object
0x68	TX_BUF_OBJ6_BYTE_0	7:0	TX_OBJ6_0	0	RW	Byte 0 (bits 7..0) of 6st data object
0x69	TX_BUF_OBJ6_BYTE_1	7:0	TX_OBJ6_1	0	RW	Byte 1 (bits 15..8) of 6st data object
0x6A	TX_BUF_OBJ6_BYTE_2	7:0	TX_OBJ6_2	0	RW	Byte 2 (bits 23..16) of 6st data object
0x6B	TX_BUF_OBJ6_BYTE_3	7:0	TX_OBJ6_3	0	RW	Byte 3 (bits 31..24) of 6st data object
0x6C	TX_BUF_OBJ7_BYTE_0	7:0	TX_OBJ7_0	0	RW	Byte 0 (bits 7..0) of 7st data object
0x6D	TX_BUF_OBJ7_BYTE_1	7:0	TX_OBJ7_1	0	RW	Byte 1 (bits 15..8) of 7st data object
0x6E	TX_BUF_OBJ7_BYTE_2	7:0	TX_OBJ7_2	0	RW	Byte 2 (bits 23..16) of 7st data object
0x6F	TX_BUF_OBJ7_BYTE_3	7:0	TX_OBJ7_3	0	RW	Byte 3 (bits 31..24) of 7st data object
0x72	VBUS_SINK_DISCONNECT_THRESHOLD_L	7:0	VBUS_SINK_DISCNT_THD[7:0]	0	R	Not support
0x73	VBUS_SINK_DISCONNECT_THRESHOLD_H	7:2	Reserved	0	R	
		1:0	VBUS_SINK_DISCNT_THD[9:8]	0	R	Not support
0x74	VBUS_STOP_DISCHARGE_THRESHOLD_L	7:0	VBUS_STOP_DISCHG_THD[7:0]	0	R	Not support
0x75	VBUS_STOP_DISCHARGE_THRESHOLD_H	7:2	Reserved	0	R	
		1:0	VBUS_STOP_DISCHG_THD[9:8]	0	R	Not support
0x76	VBUS_VOLTAGE_ALARM_HI_L	7:0	VBUS_VOLTAGE_ALARM_HI[7:0]	0	R	Not support
0x77	VBUS_VOLTAGE_ALARM_HI_H	7:2	Reserved	0	R	
		1:0	VBUS_VOLTAGE_ALARM_HI[9:8]	0	R	Not support
0x78	VBUS_VOLTAGE_ALARM_LO_L	7:0	VBUS_VOLTAGE_ALARM_LO[7:0]	0	R	Not support
0x79	VBUS_VOLTAGE_ALARM_LO_H	7:2	Reserved	0	R	
		1:0	VBUS_VOLTAGE_ALARM_LO[9:8]	0	R	Not support

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Address	Reg Name	Bit	Bit Name	Default	Type	Description
0x9B	SYS_CTRL8	7	CK_300K_SEL	1	RW	1: 300K divided from BMCIO_24M 0: 320K from BMCIO_320K
		6	Reserved	1	R	
		5	SHIPPING_OFF	0	RW	0: Shipping mode 1: Non-shipping mode
		4	ENEXTMSG	0	RW	0: Disable PD3.0 Extended message 1: Enable PD3.0 Extended message affect GoodCRC receive detect between PD2.0 and PD3.0
		3	AUTOIDLE_EN	0	RW	1: Auto enter idle mode enable 0: Auto enter idle mode disable
		2:0	AUTOIDLE_TIMEOUT	000	RW	Enter idle mode timeout time = (AUTOIDLE_TIMEOUT*2+1)*6.4ms

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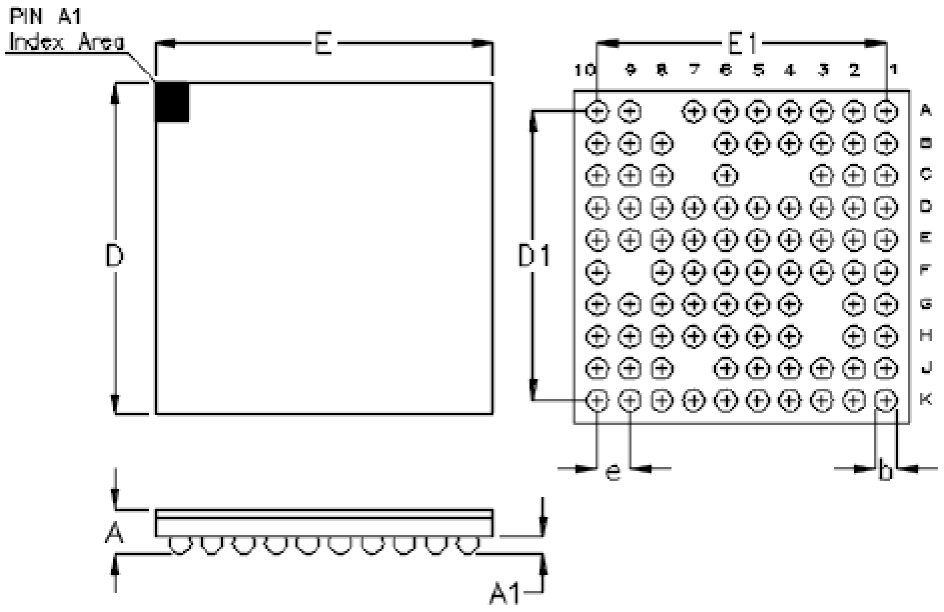
5 MT6371 Packaging

5.1 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	4.100	4.180	0.161	0.165
D1	3.600		0.142	
E	4.180	4.260	0.165	0.168
E1	3.600		0.142	
e	0.400		0.016	

91B WL-CSP 4.22x4.14 Package (BSC)

Figure 5-1. Package dimension

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Appendix

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